National Applied Research Laboratories

New Paradigm of Nano Device: From More Moore to More than Moore

Wen-Kuan Yeh

Director General

Nano Device Laboratories, Taiwan

Outline

1. Background
2. More Moore
3. More than Moore
4. NDL introduction

The Transistor Revolution (1)

The First Transistor

1947 Bell labs.

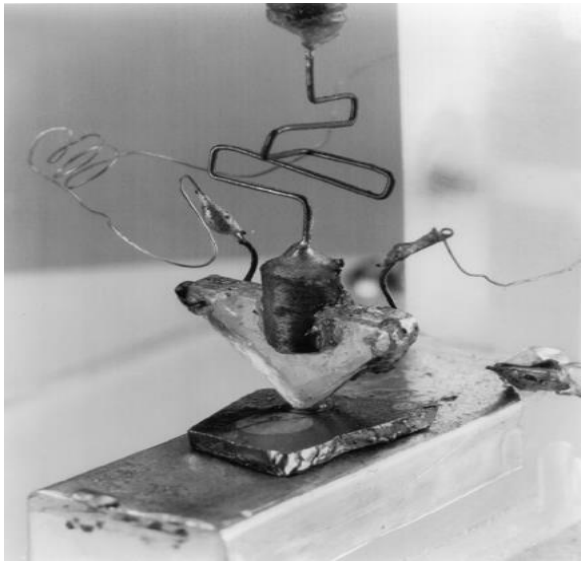


FIG. 1. The first transistor. Brattain and Bardeen's pnp point-contact germanium transistor operated as a speech amplifier with a power gain of 18 on December 23, 1947. (***Bell Labs, Lucent***)

The UMC 0.25um Transistor

1999, UMC

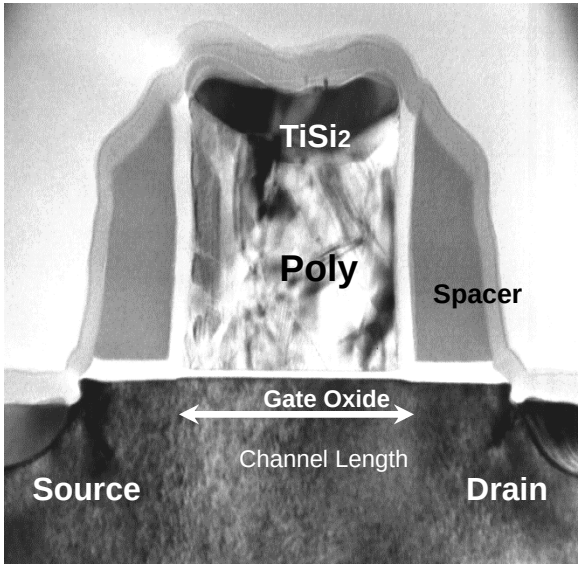


FIG. 2. The UMC post generation 0.25um standard transistor (***UMC***)

The worldwide leadship

2007 Intel

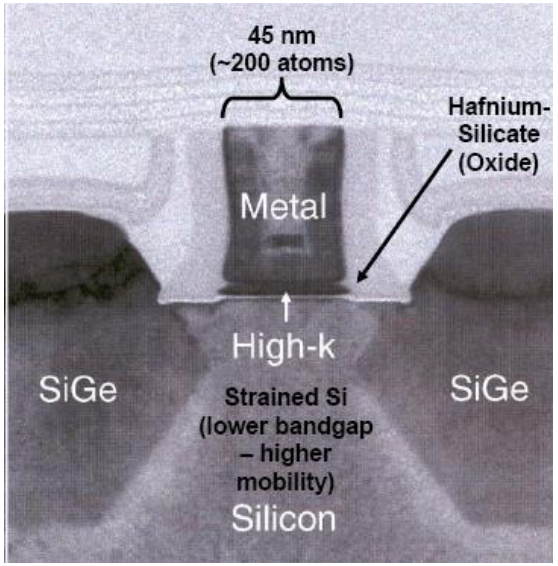
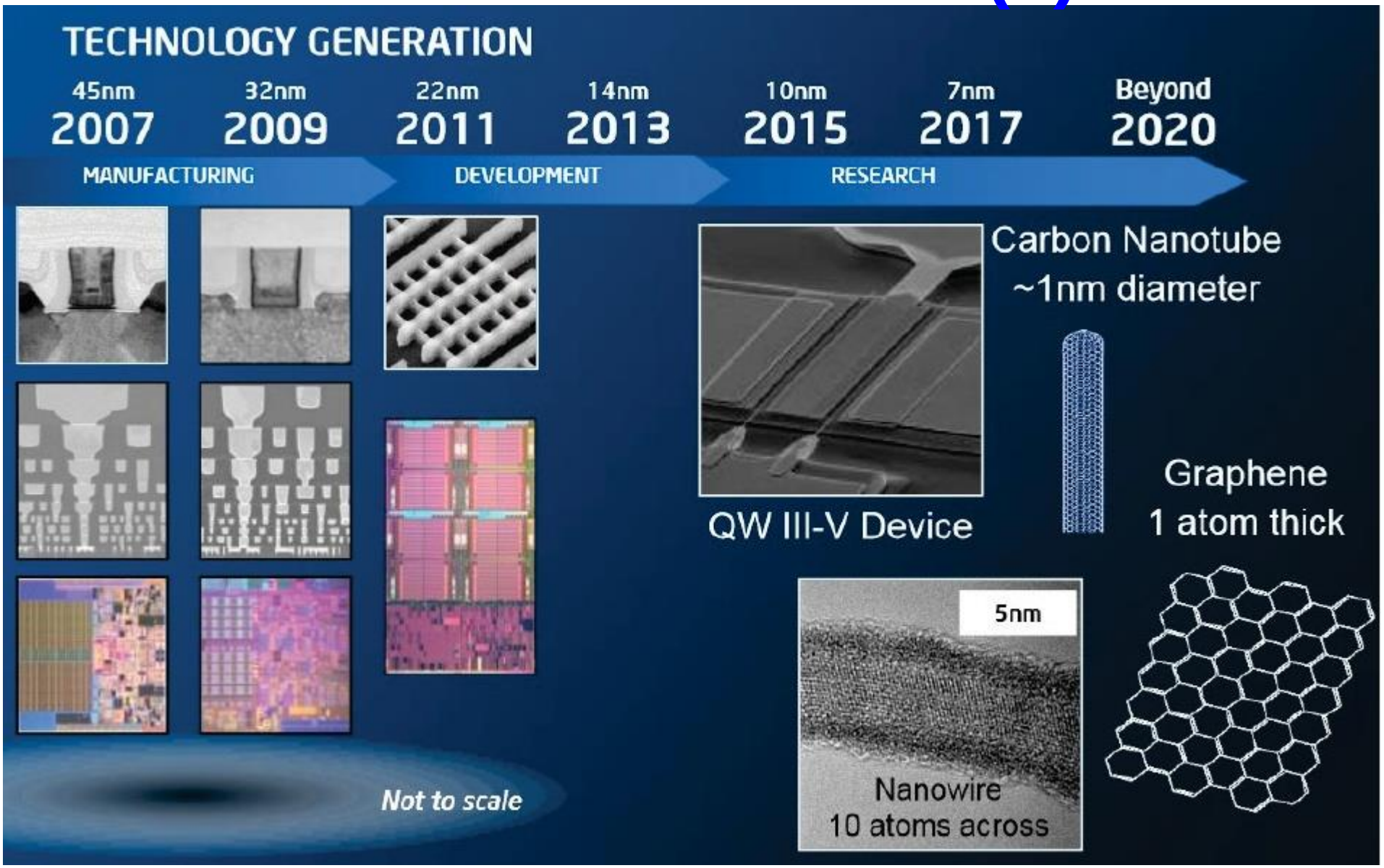


FIG. 3. The worldwide smallest transistor Gate length 0.045 um. (***INTEL, CPU)***

Keep Structure but Replacing Material!

The Transistor Revolution (2)



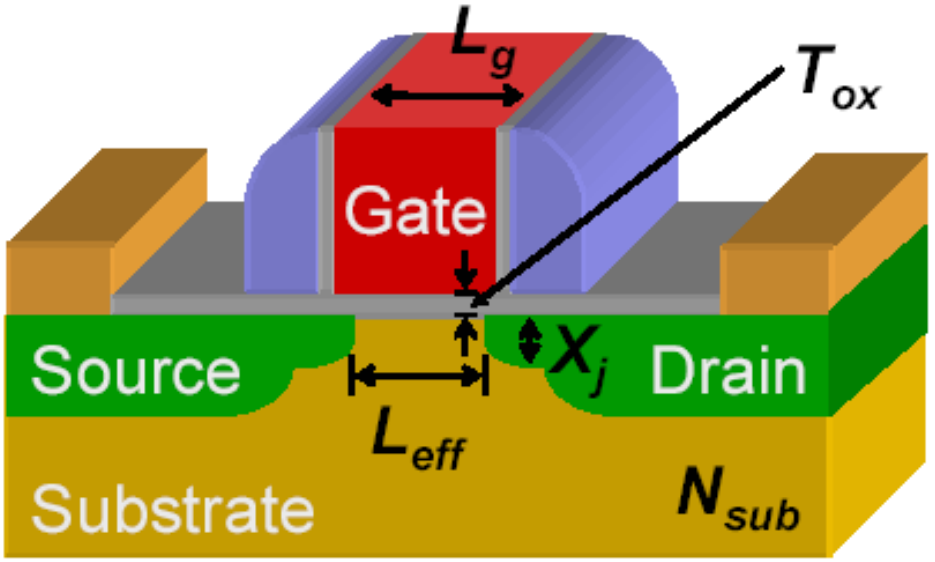
Alternative Structure and Material! *Source: INTEL*

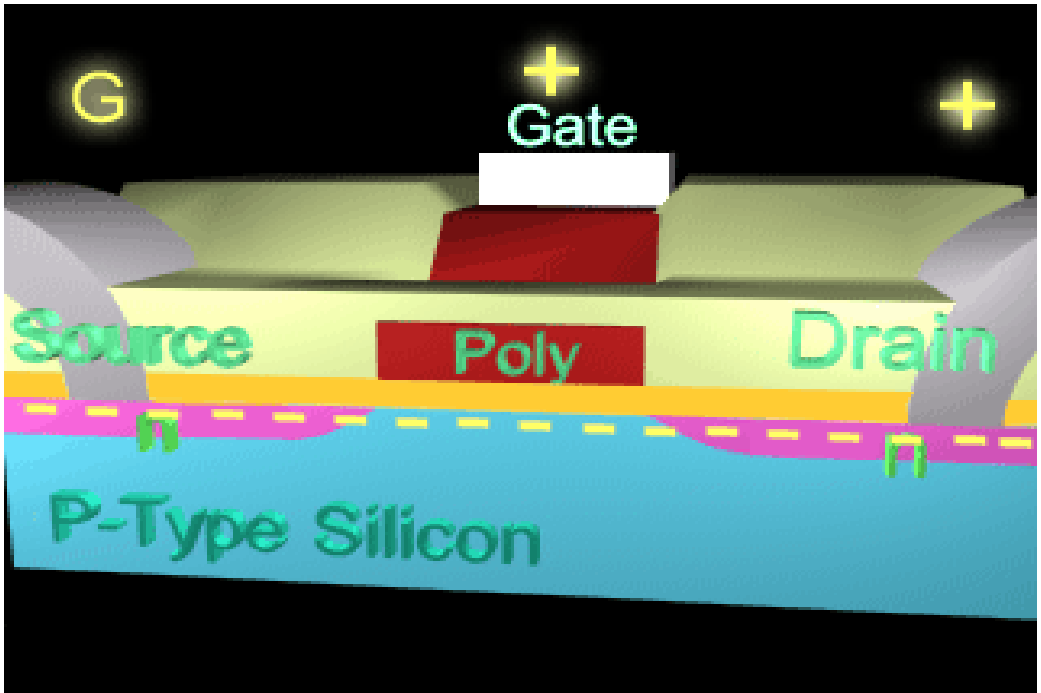
Planar MOSFET

Bulk-Si MOSFET:

Desired characteristics

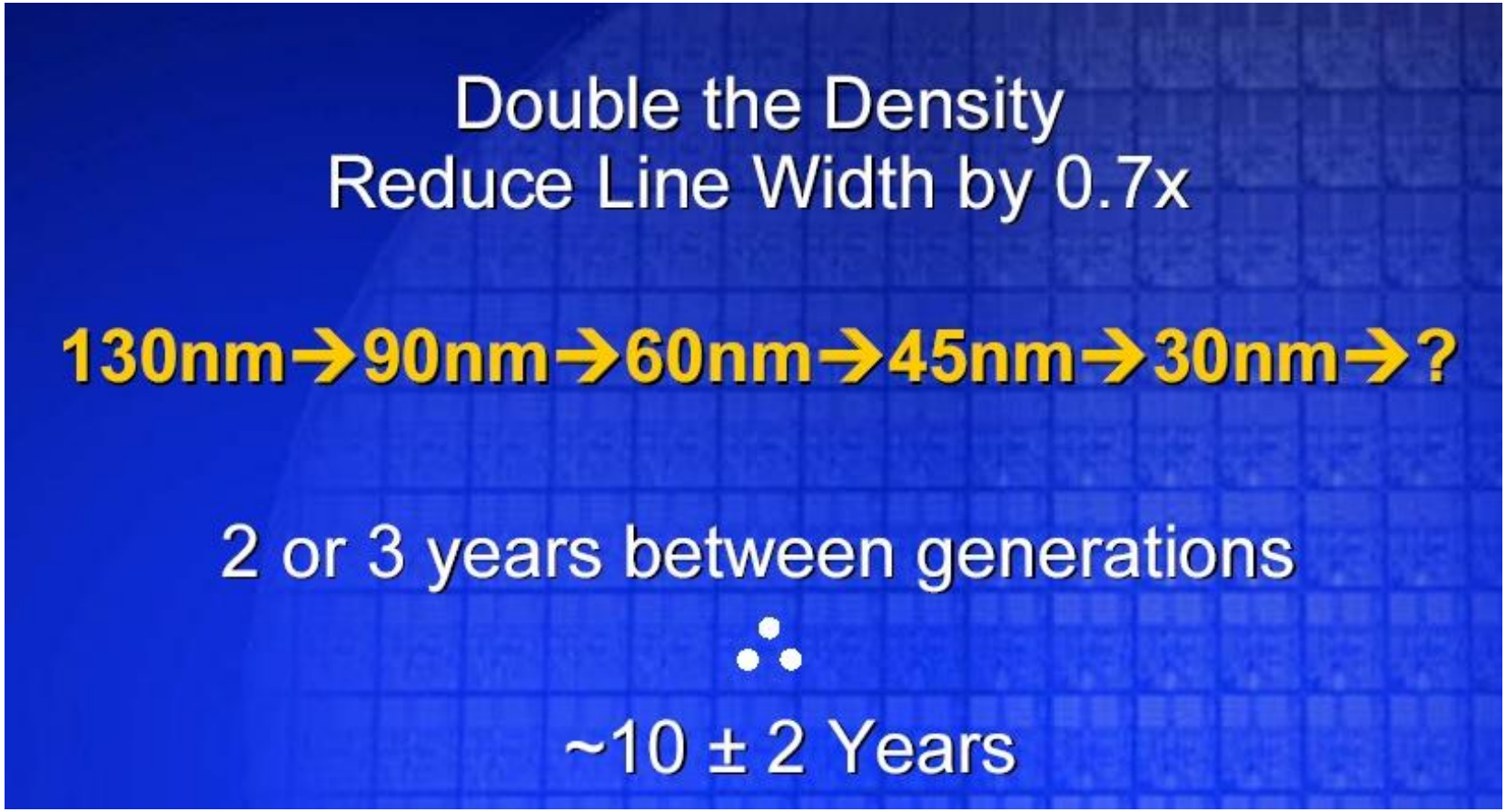
- High ON current (I_{dsat})
- Low OFF current





Nano 2016, W-K Yeh

Moore's Law



Source : G. E. Moore

Background in Semiconductor Study (1990-2016)

- 1988 ~ 1990: Master of EE degree in NCKU (1.2um $TiSi_2$ Salicidation), also join tsmc TD in Fab. I.
- 1992 ~ 1996: PhD of EE degree in NCTU (0.5 um Selective CVD Tungsten), also join NDL with collaboration with tsmc Fab 4.
- 1996 ~ 2000: join ATD in UMC (develop 0.25um, 0.18um, 0.13um MOSFET, and 90nm SOI MOSFET)
- 2000 ~ join start up of EE department in National university of Kaohsiung. Elected as Chair of EE Department, Dean of Engineering. (with collaboration with tsmc/UMC in 90nm, 65nm, 45nm, and 28nm MOSFET)
- 2014 ~ General director of NDL (focus on 7-5nm device development)

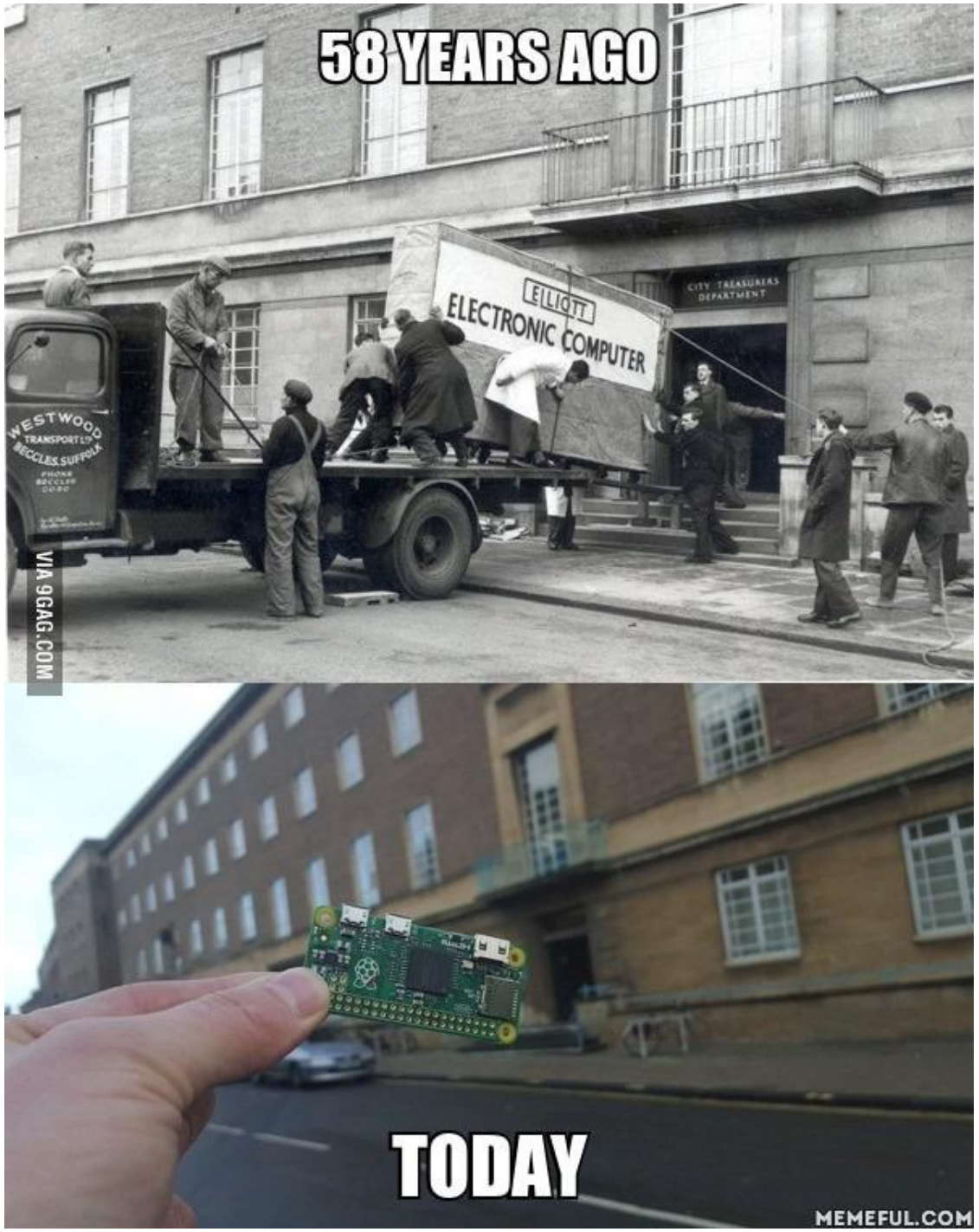
Device

↓

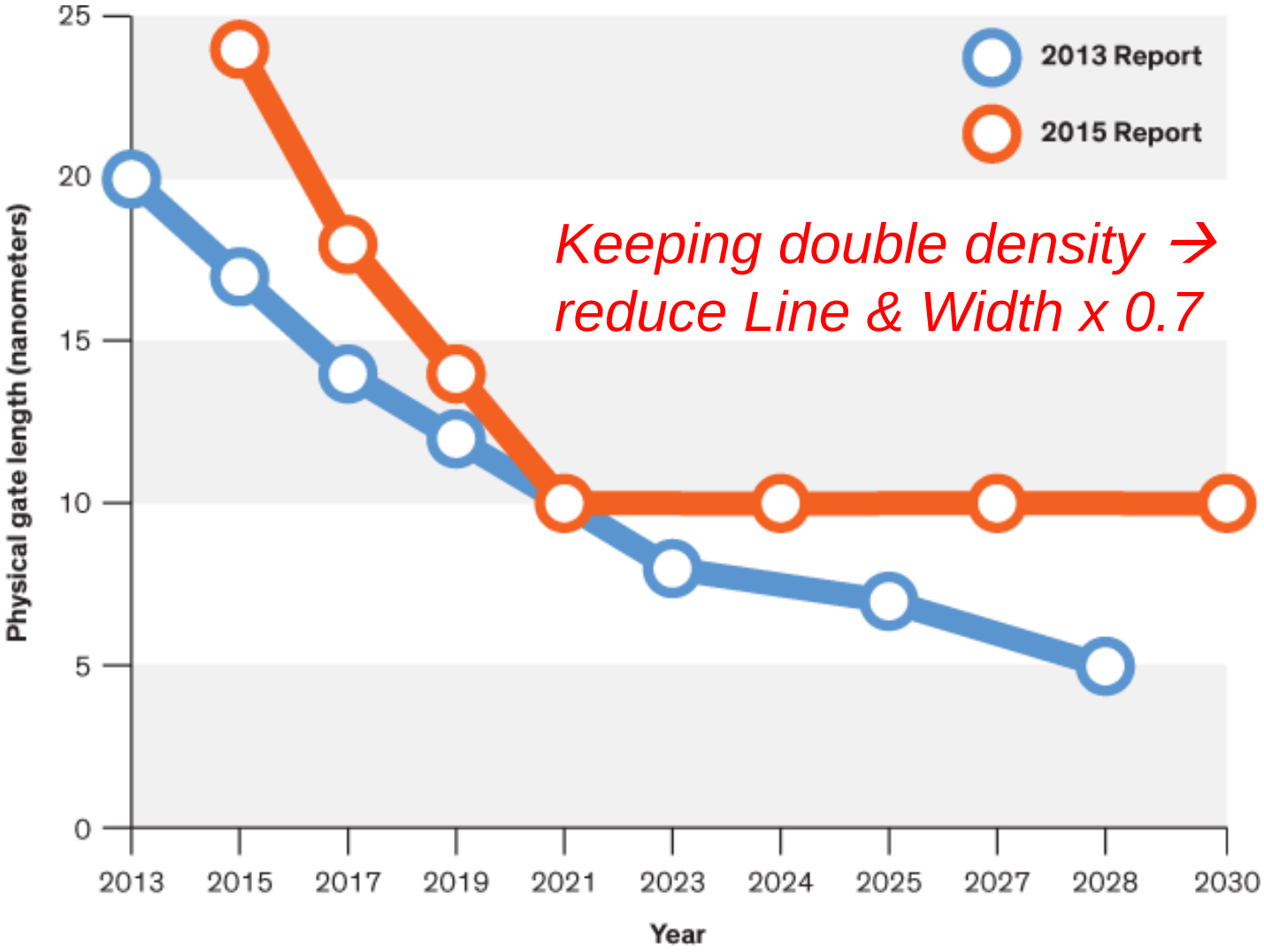
x1/200

58 years Device Scaling Impact!

58 years on, Norwich City Hall finally gets a new computer



Moore's Law to the end?

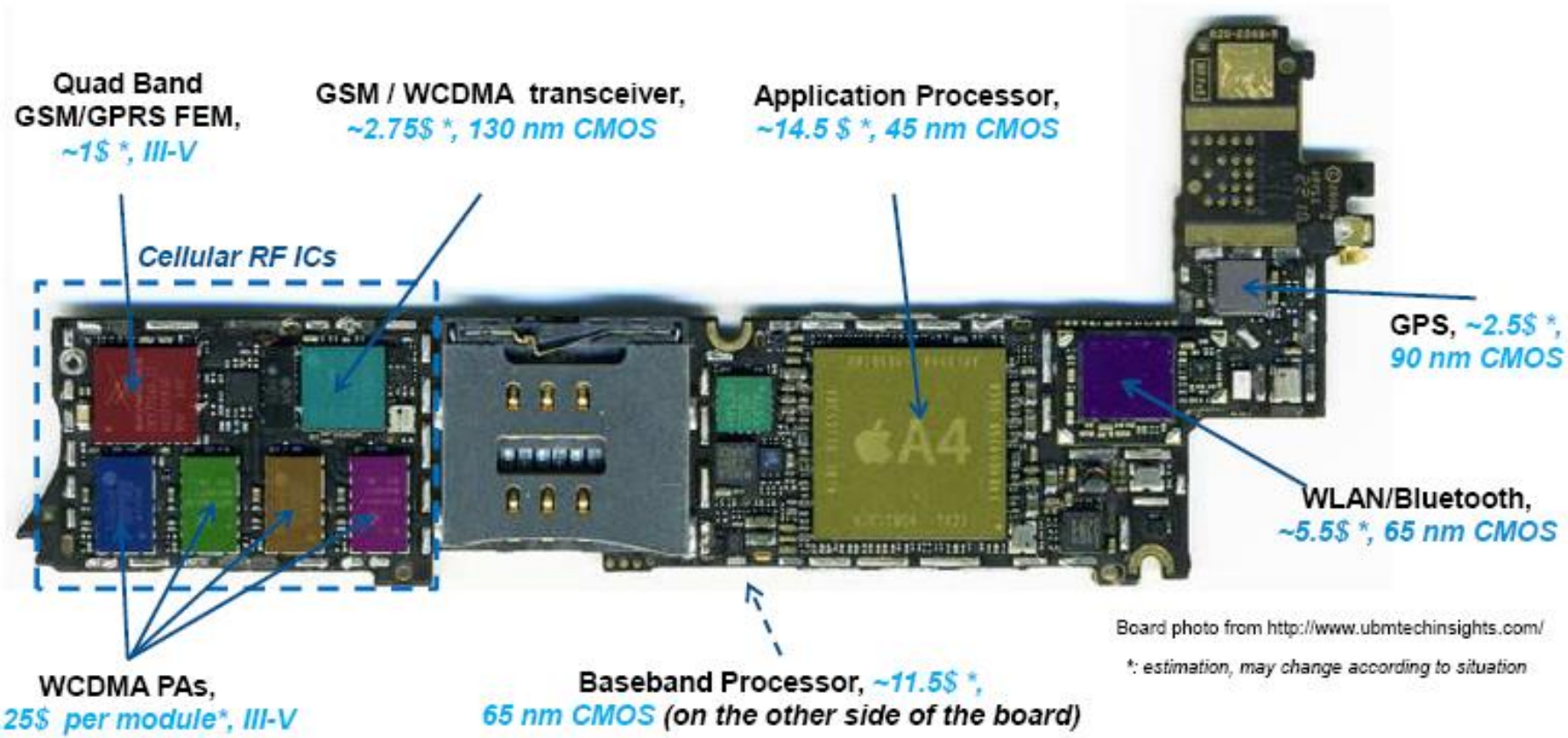


Nano 2016, W-K Yeh

Erik Vrielink

Tablet Smart Phone

Apple iPhone 4 Teardown:



i Phone Image Signal Processor

A6-A7

Samsung 28nm planar CMOSFET

↓

A8

tsmc 20nm planar CMOSFET

↓

A9

tsmc 16nm FinFET CMOSFET

Samung 14nm FinFET CMOSFET

↓

A10

tsmc 10nm FinFET CMOSFET

i Phone 6s

A9 Image Signal Processor

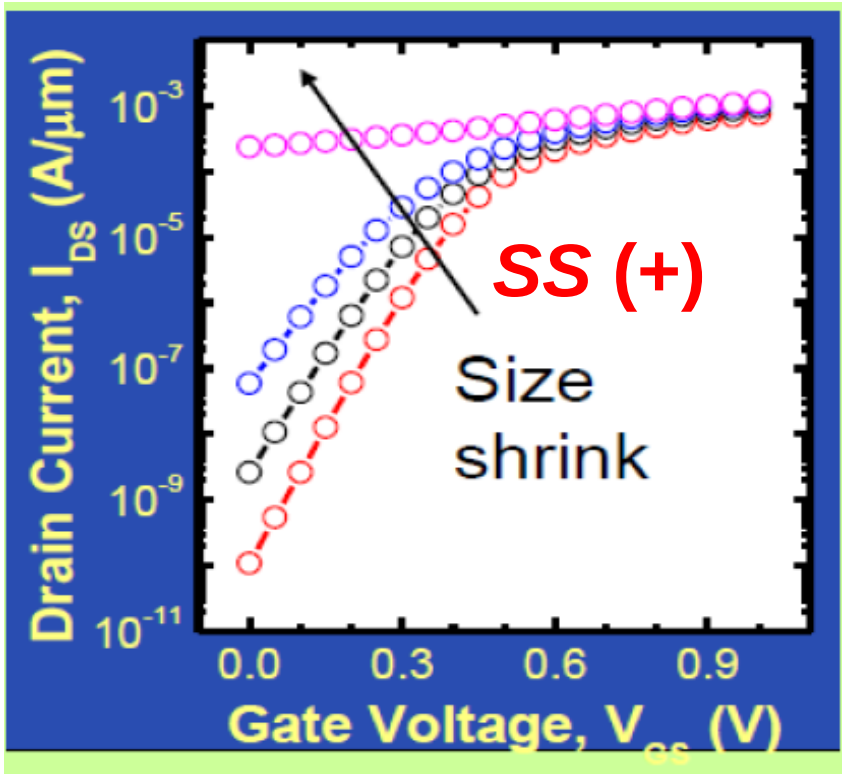
tsmc 16nm FinFET, Samung 14nm FinFET

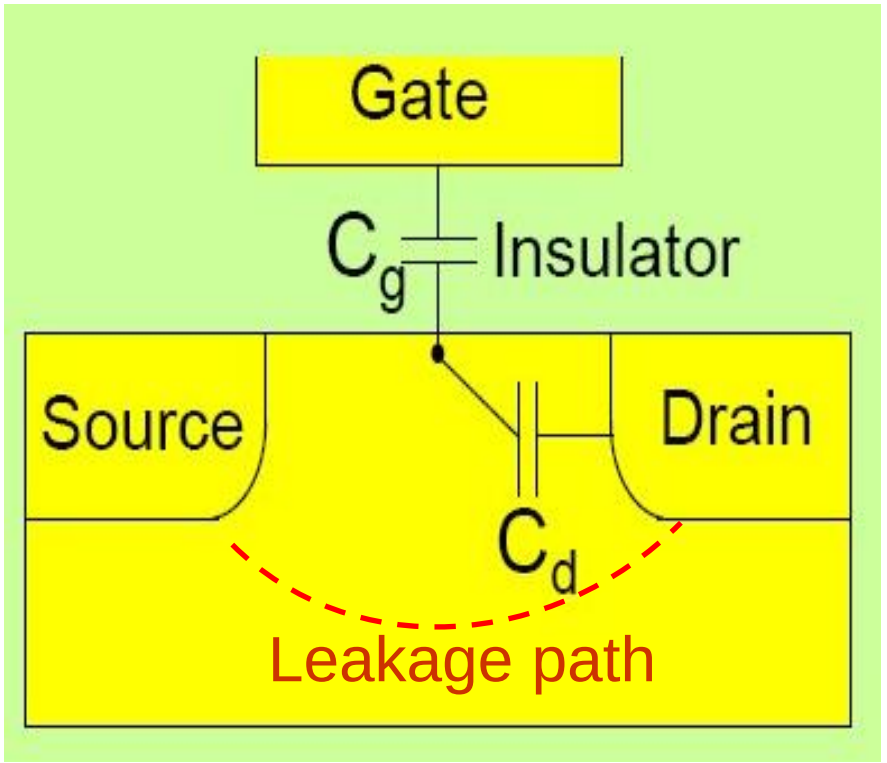
i Phone 7

A10 Image Signal Processor

tsmc 16nm FinFET

Planar Bulk Si MOSFET reach to limit





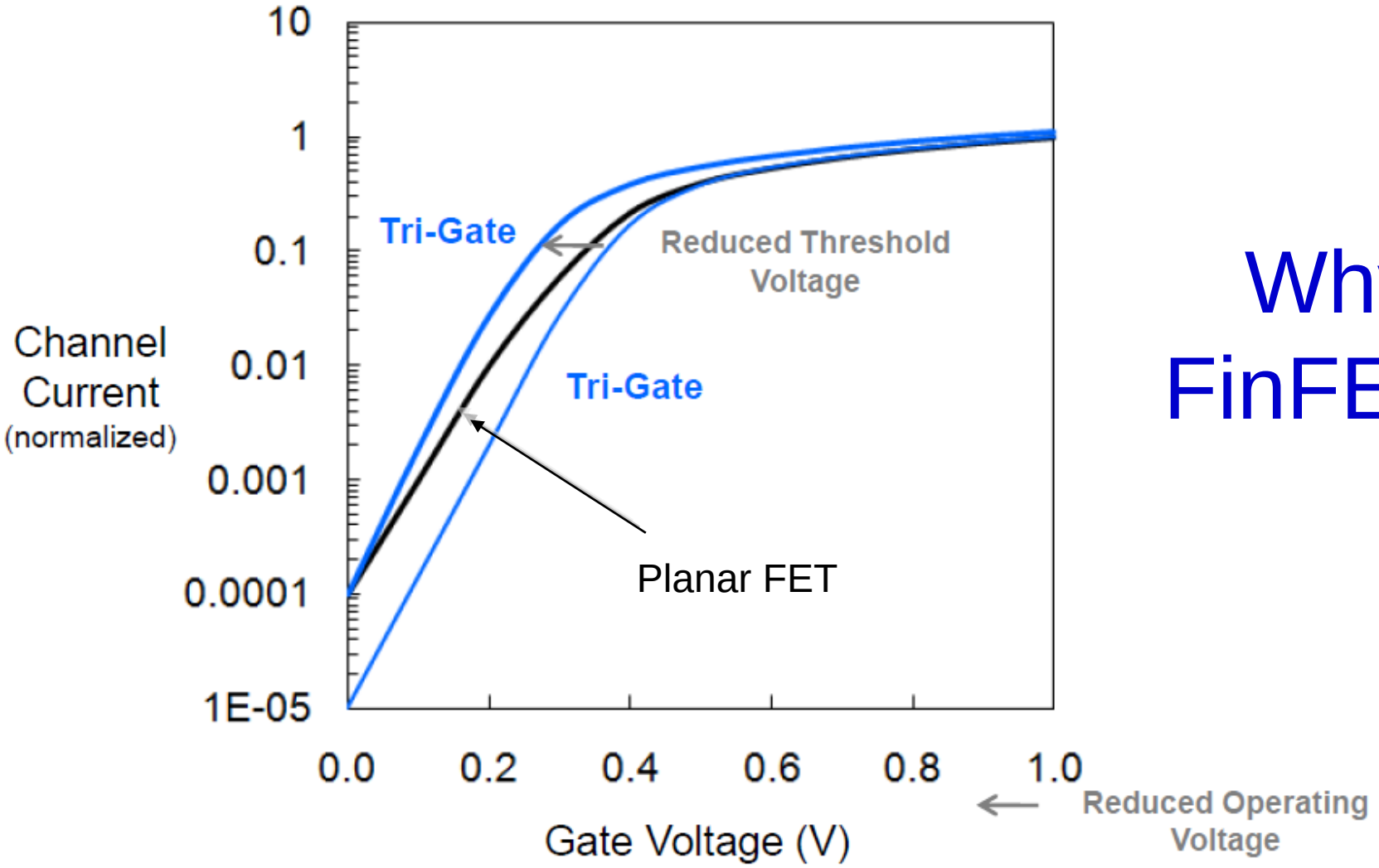
$SS \sim 60mV(1+C_{dm}/C_{ox})$

Reducing EOT to increase C_{ox} is not enough to keep gate control !
Drain become dominate control in channel barrier!

But !!

Big subthreshold swing!
It is difficult to scaling following Moore's Law!

Source: Chenming Hu, July 2011



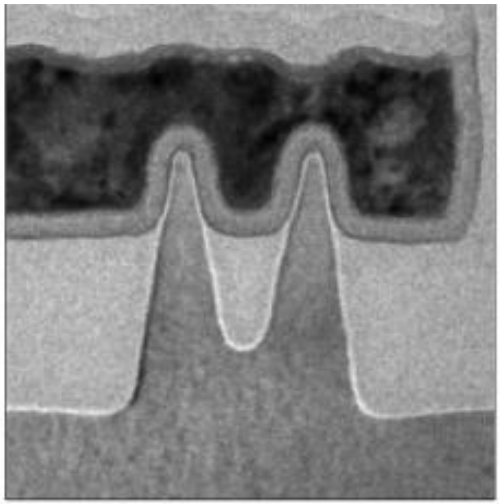
Why FinFET?

The steeper sub-threshold slope can also be used to target a lower threshold voltage, allowing the transistors to operate at lower voltage to reduce power and/or improve switching speed

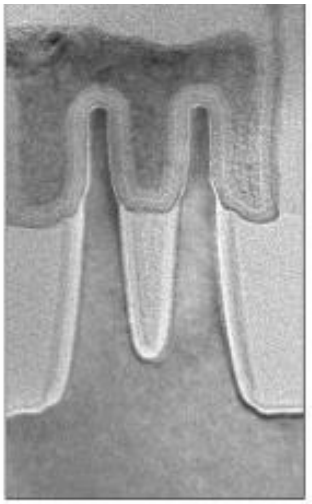
Source: INTEL 2012

tsmc vs. INTEL and Samsung

INTEL
14 nm FinFET

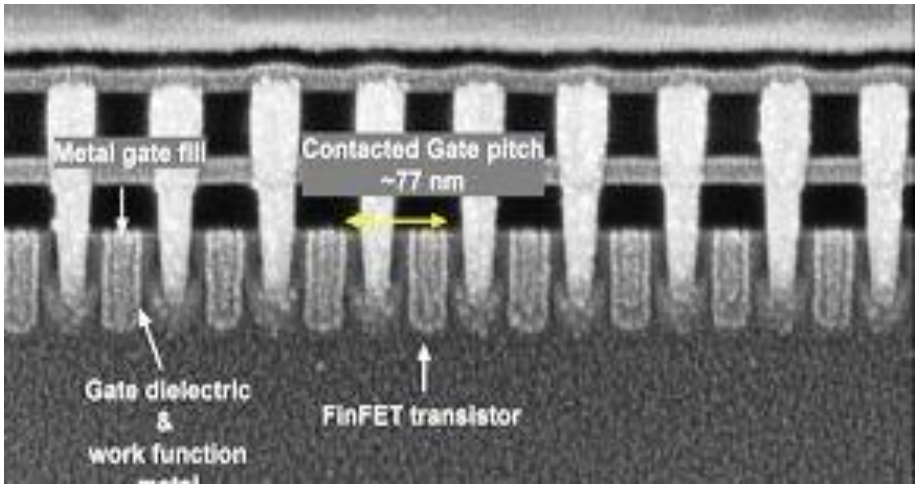


22 nm 1st Generation
Tri-gate Transistor

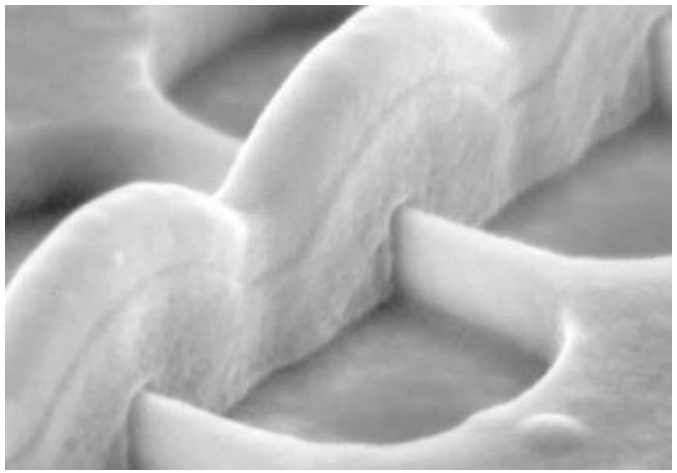


14 nm 2nd Generation
Tri-gate Transistor

Samsung 14 nm FinFET



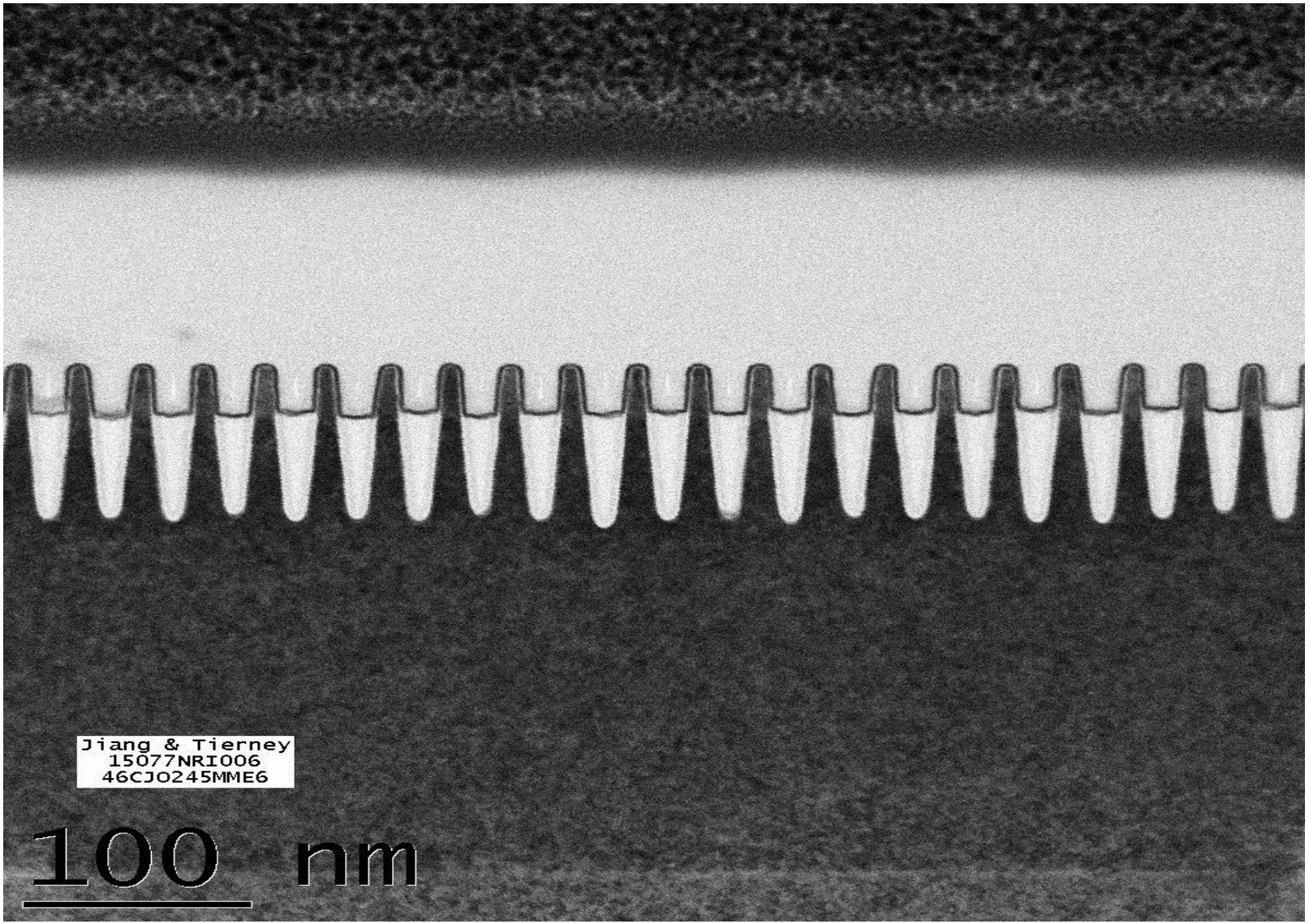
TSMC 16 nm FinFET



Nano 2016, W-K Yeh

Source: INTEL 2014, tsmc 2014, Samsung 2015

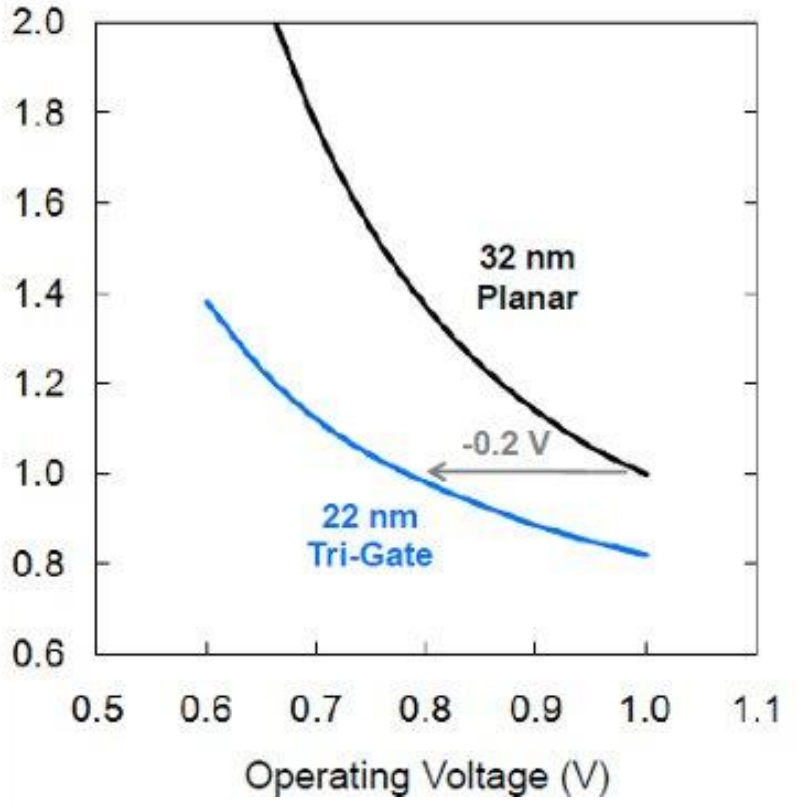
IBM 7nm FinFET



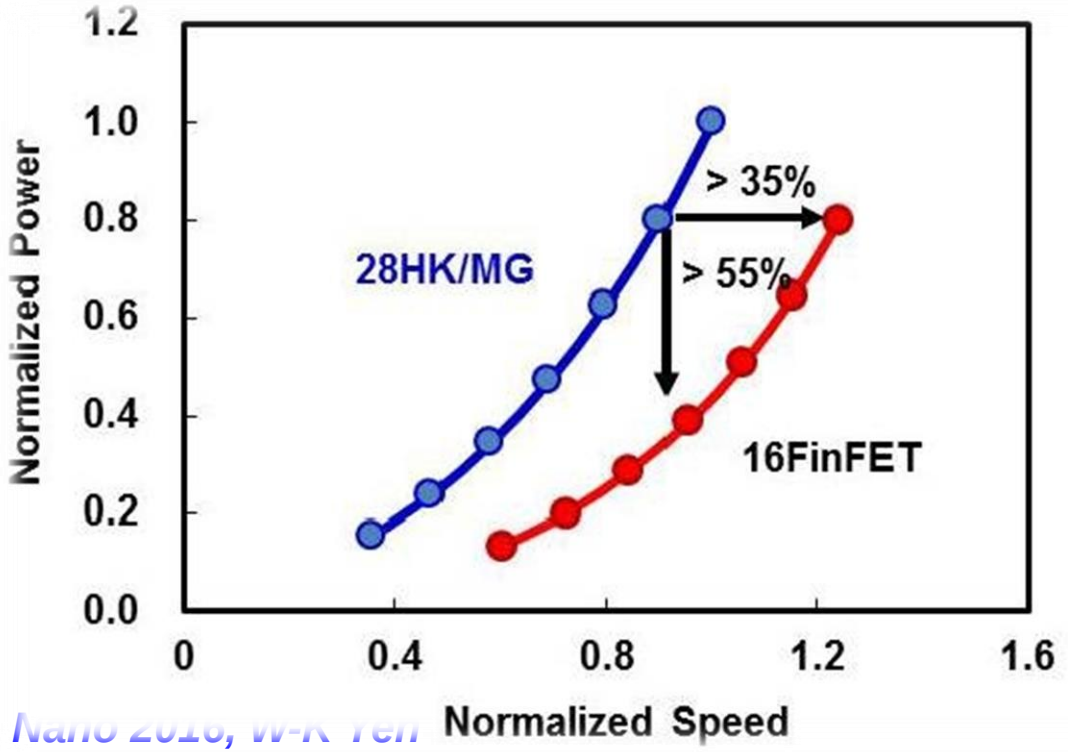
Bulk 7nm transistors, with a 30nm pitch (the distance between the front edge of one transistor and the front edge of the next transistor). IBM Research

tsmc vs. INTEL

INTEL 22nm FinFET



tsmc 16nm FinFET



Intel Shows 14nm Broadwell Consuming 30% Less Power Than 22nm Haswell !!

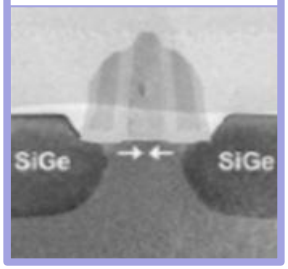
Source: INTEL 2011, tsmc 2013

Nano Device Trend

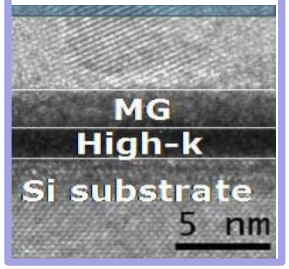
2003 2007 2011 2015 2019

16-10 nm 7-5 nm

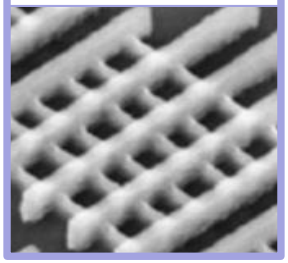
90 nm



45 nm



22/20 nm

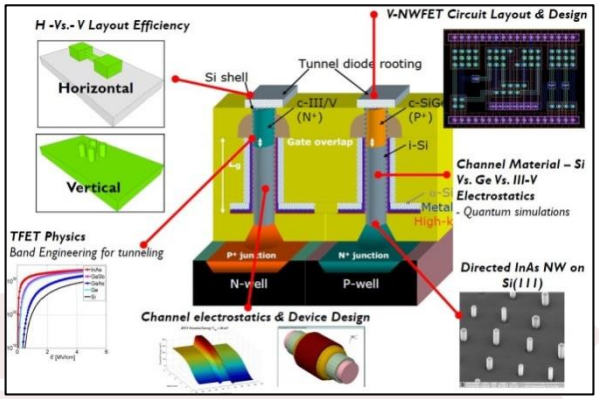


Strain Technology

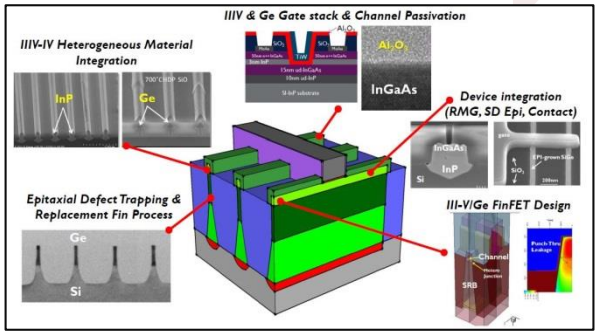
High-K Metal Gate

3D FET

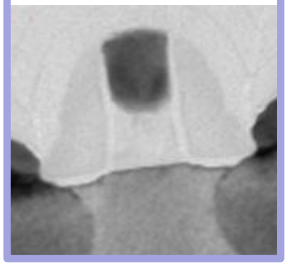
New Structure ??



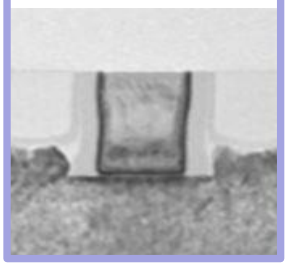
New Material ??



65 nm



32 nm



Nano 2016, W-K Yeh

From FinFET (n=2~3) to nanrwire (n=4)

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{n\,\varepsilon_{Ox}} t_{Ox} W_{Si}}$$

$$L_{eff} > 6\,\lambda$$

$$L_G \sim 1.5 W_{fin}$$

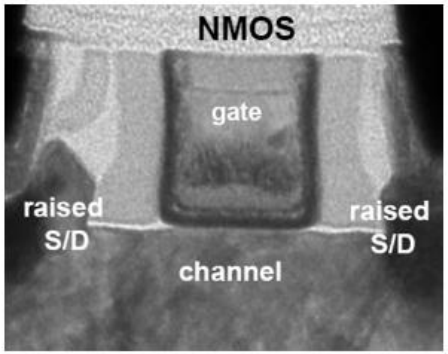
$$H_{fin} \leq L_G$$

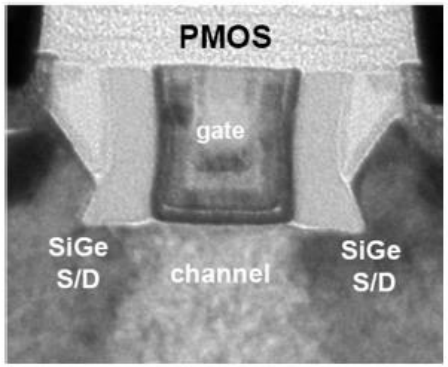
- Only for channel length 3-4 times larger than the fin thickness , scaling rules are correctly fulfilled and *SS* parameter has a reasonably low value (60-80).
- Short channel effects can be avoided by reducing the fin thickness (**W_{Si}**) or by reducing the gate oxide thickness (**t_{Ox}**).
- **natural length** parameter **lambda** is improved by increasing the number **n of gates** or by increasing the gate oxide dielectric constant.

Alternative Device Structure

Planar → FinFET → Gate-all-around FETs

32 nm
planar

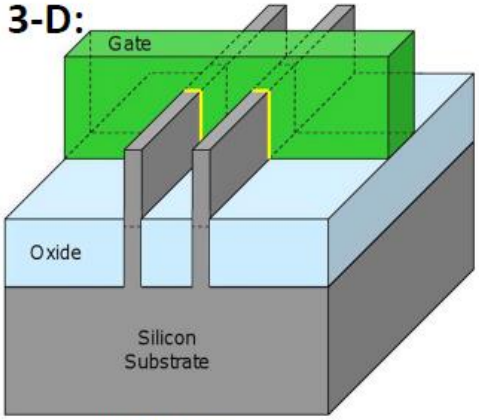




P. Packan *et al.* (Intel), *IEDM* 2009

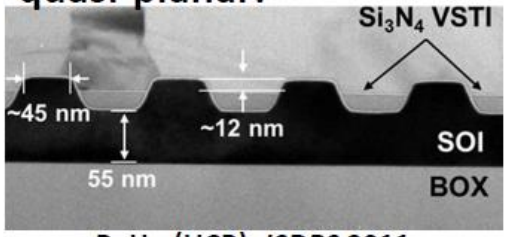
22 nm
multi-gate
segmented channel

3-D:



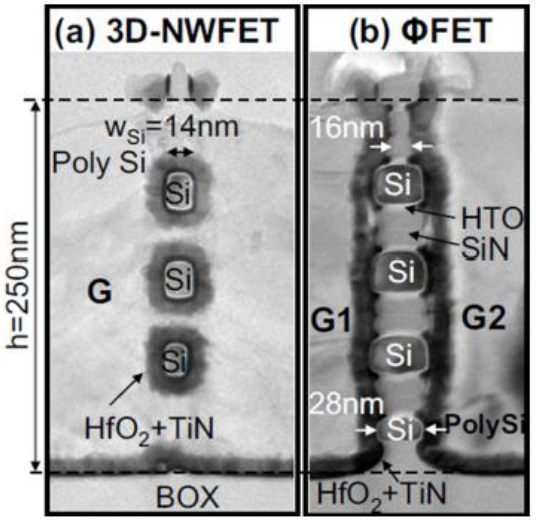
Intel Corp.

quasi-planar:



B. Ho (UCB), *ISDRS* 2011

beyond 10 nm
stacked nanowires



C. Dupré *et al.* (CEA-LETI) *IEDM* 2008

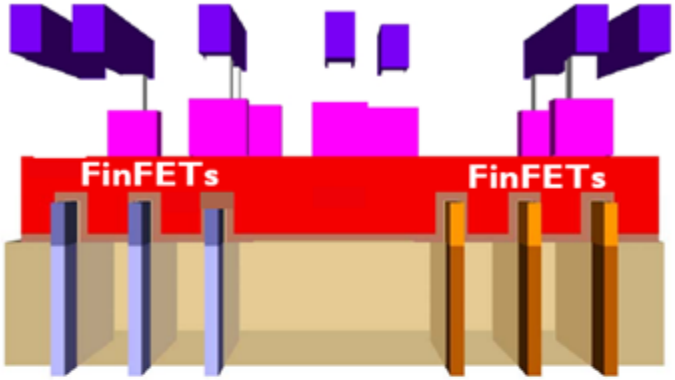
Stacked gate-all-around (GAA) FETs achieve the highest layout efficiency.

one gate → 2, 3 Gates → ≥ 4 Gates

Nano 2016, W-K Yeh

Alternative Material

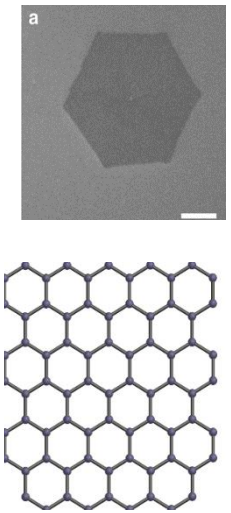
Si → Ge → III-V → 2D / Graphene



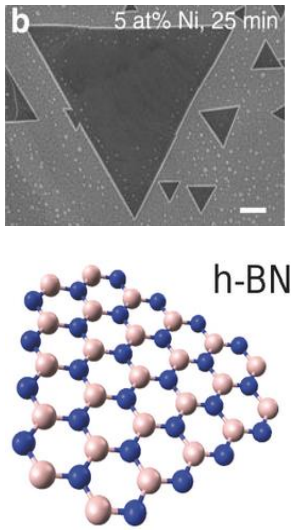
	Hole mobility (cm2/Vs)	Electron mobility (cm2/Vs)
Si	430	1600
Ge	**3900**	3900
GaAs	400	**9200**
InAs	500	40000

(high mobility channel)

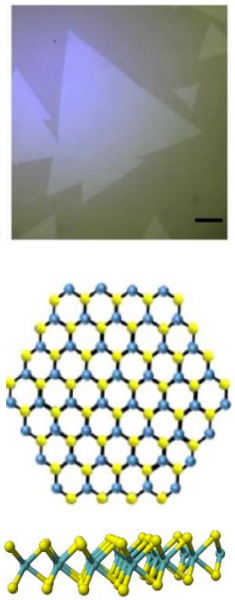
Graphene



h-Boron Nitride



Transition Metal Dichalcogonide



(ultra thin body channel)

Nano 2016, W-K Yeh

[Ref. 1] K. S. Novoselov, et al, Electric Field Effect in Atomically Thin Carbon Films, Science, 306, 666 (2004)
[Ref. 2] A. C. Ferrari, et al, Raman Spectrum of Graphene and Graphene Layers, Phy. Rev. Lett., 97, 187401 (2006)

Moore *vs.* More than Moore

More Moore *vs.* More than Moore

NARLabs

Heterogeneous integration technology

New Integration
New Application

More Application

Analog/RF | Passives | HV Power | Sensors Actuators | Biochips

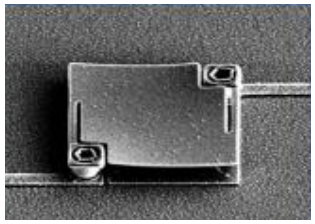
Nano fabrication technology

More Scaling

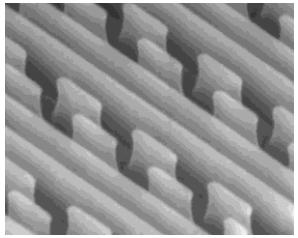
CMOS：CPU, Memory, Logic

130nm
90nm
65nm
45nm
32nm
22nm
14nm
.
.
.
小於5nm

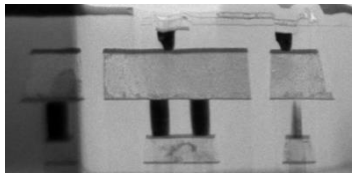
Sensor



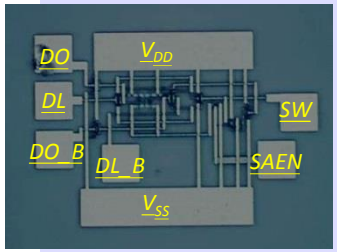
Logic Device

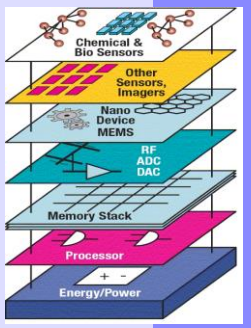


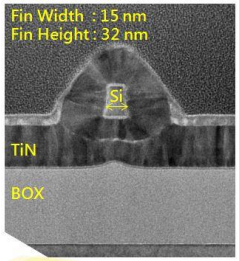
Memory Device



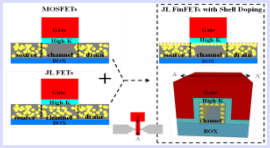
Small scale circuit



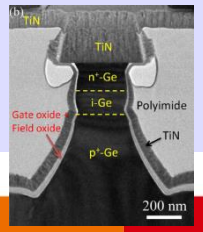


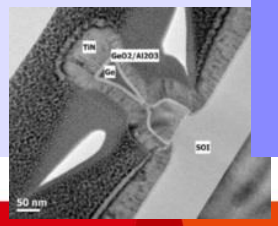


FinFET(3D)
Nanowire/GAA

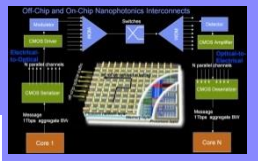


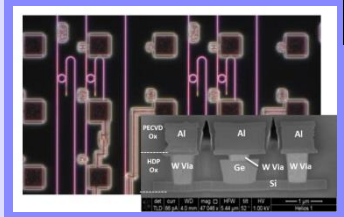
Ge(Sn), III-V, 2D, Graphene





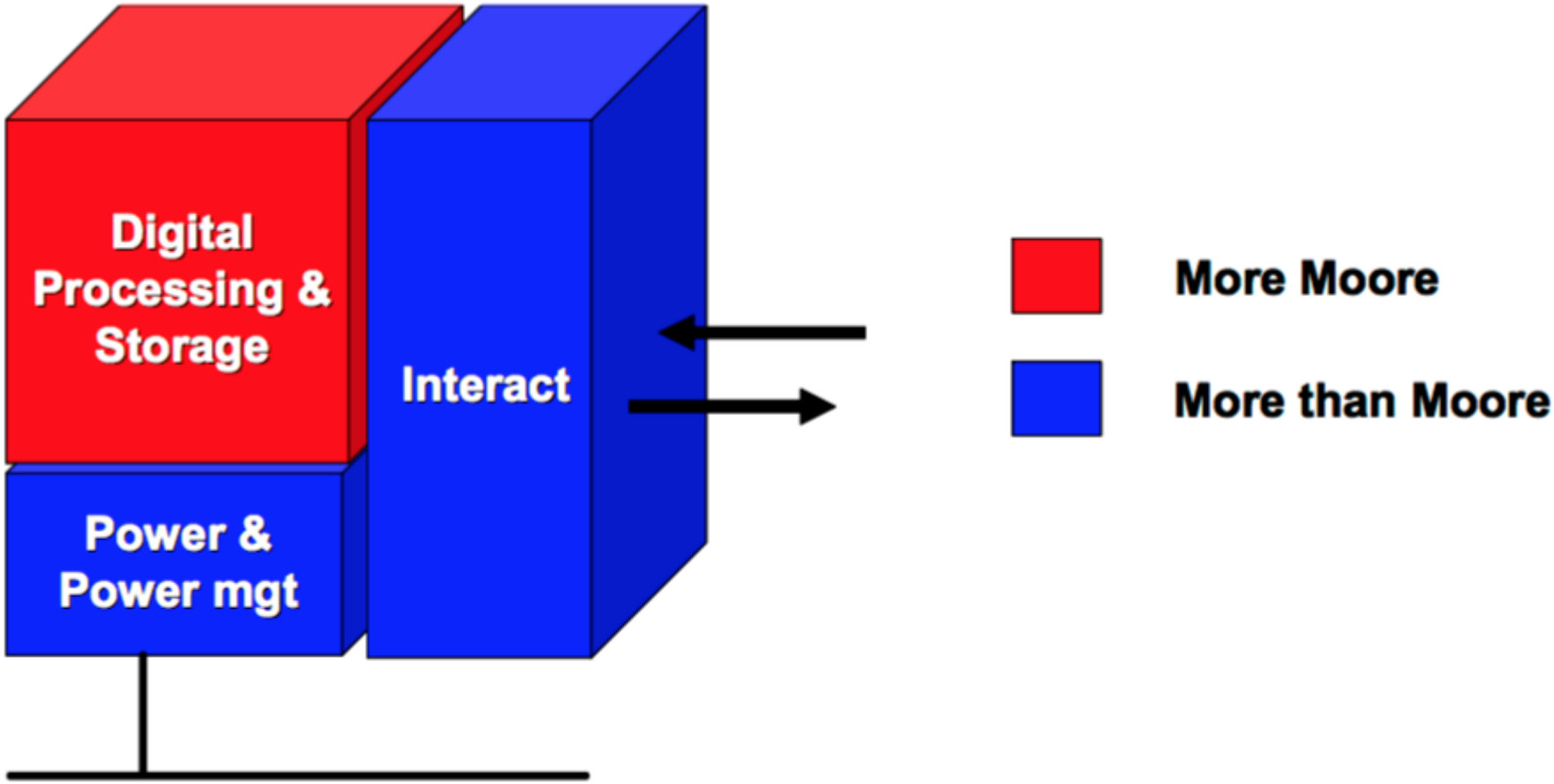
- **Post-Si chip technologies that cover cutting-edge CMOS/MEMS (bio/photonic) sensor**
- **Heterogeneous integration for IoTs**
- **Wearable electronics**
- **Biochips**





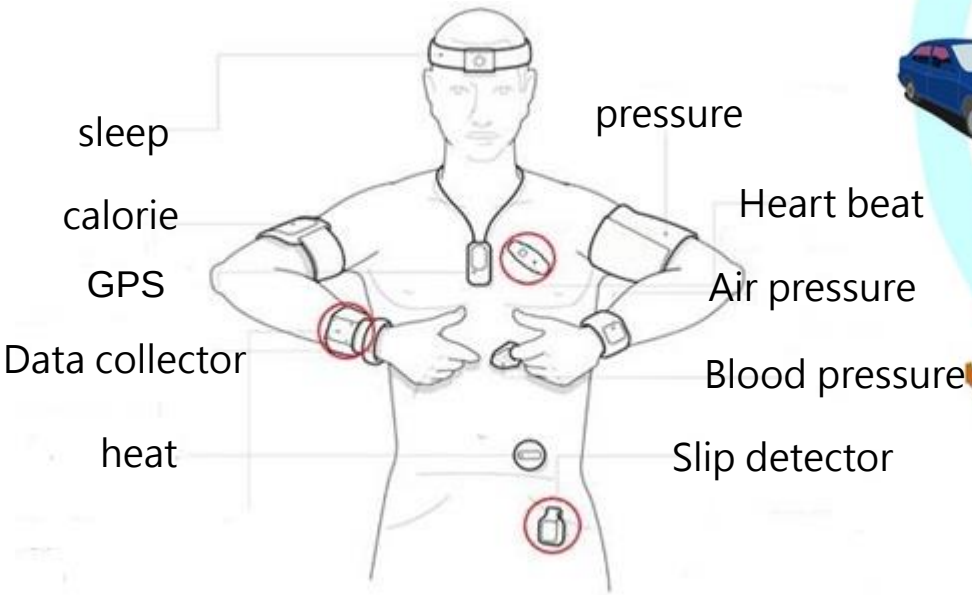
New Structure, New Material

More Moore *vs.* More than Moore



Source: 2015 International Technology Roadmap for Semiconductor

More Than Moore



Need CMOS Technology Compatible!

Source : Fujitsu Organic Energy Device Harnesses Power from In-Door Light & Heat

Internet of Things, IoT

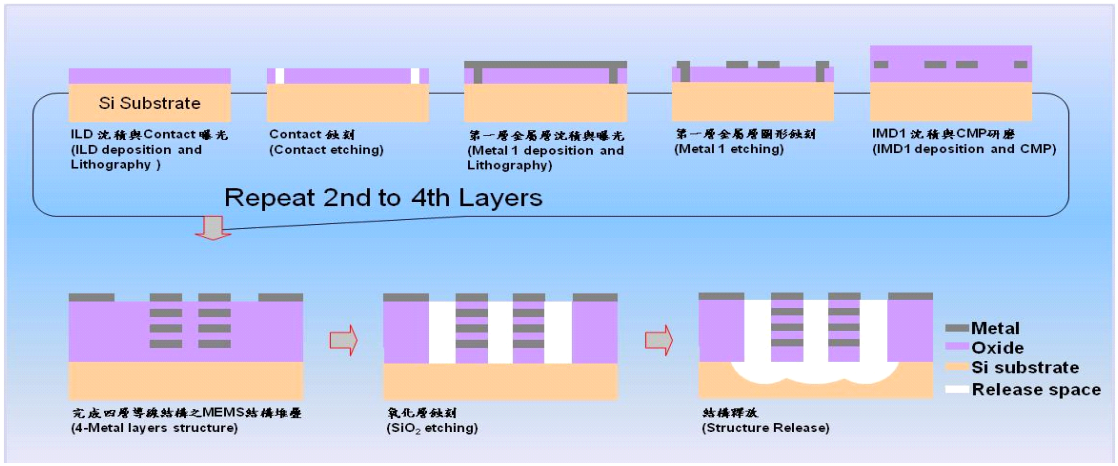
MIC predict 2016 Iot Market will be USD 620B，end product will ~ 190M.

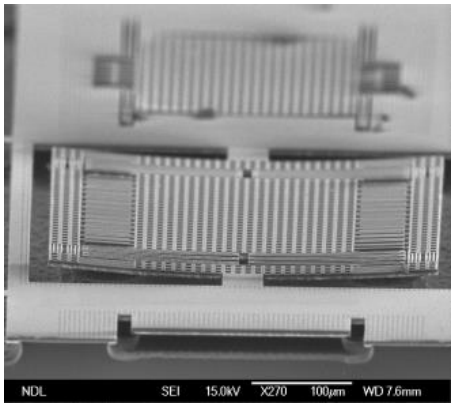
IoT requirement → Low Power, Low Cost

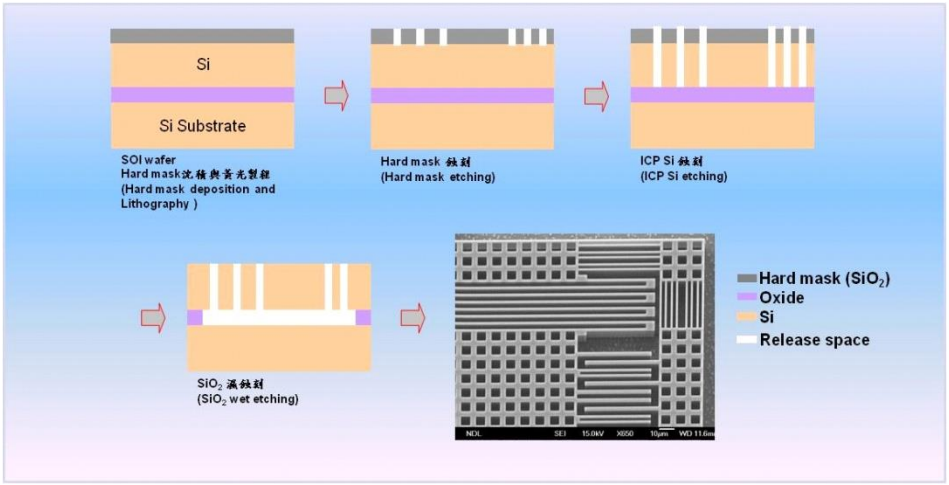
IoT Business Model

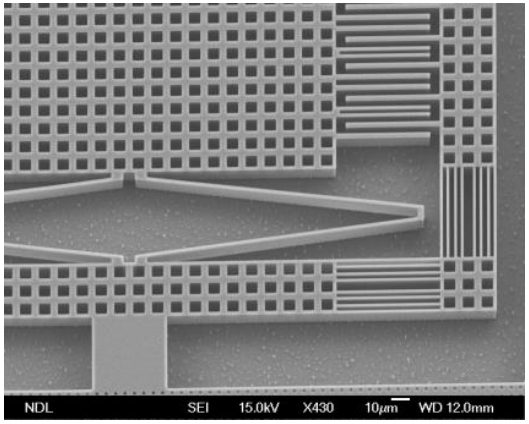
- **Sensors/MEMS**
- **Advanced package**
- **Wireless network chip**
- **High speed AP and MCU**
- **Lower power management chip**

MEMS Device Integration Platform









Silicon Compatible Process

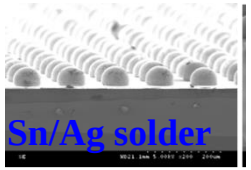
Advantage Package

System in Package (SIP)：

wafer-to-wafer、chip-to-wafer

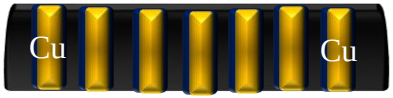
(A) Flip-Chip

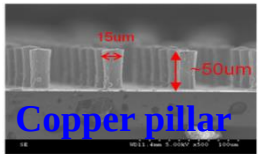
- 銅柱凸塊(CPB)
- 錫/銀球(Solder ball)

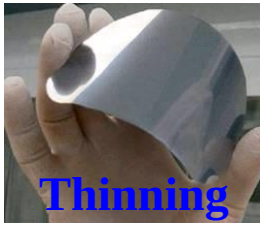


(B) TSV

- 深蝕刻矽(Deep Si etching)
- 銅晶種層/障壁層/絕緣層
- 深孔銅電鍍
- 薄化 (CMP)

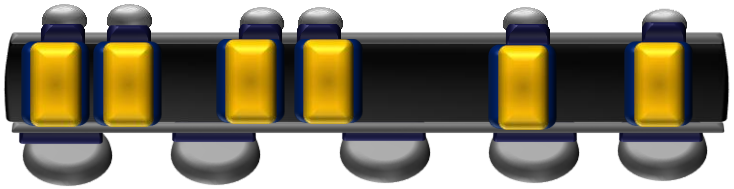




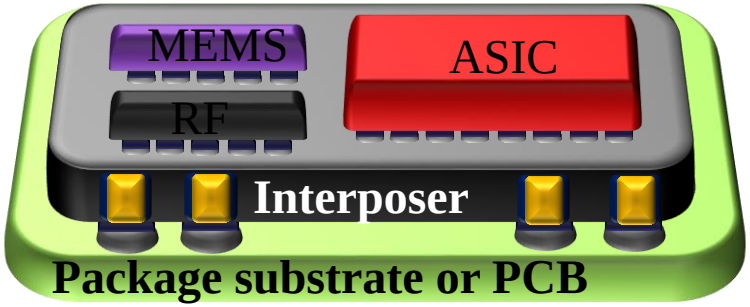


(C) interposer

- 重佈線路層(RDL；Redistribution Layer)
- 凸塊 (Bump)
- 鍵合技術 (bonding)



2.5D IC

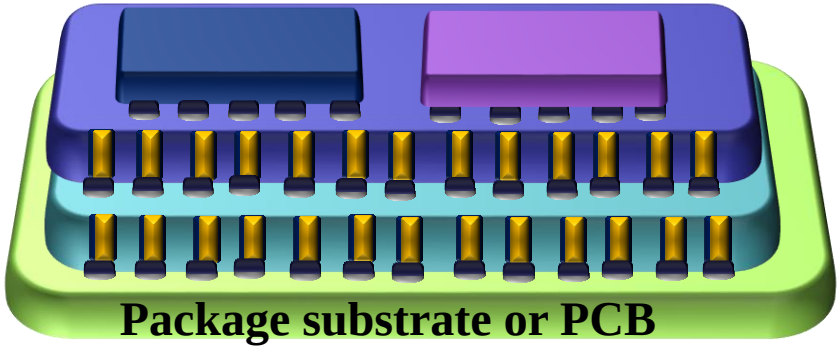


TSV

Cu pillar

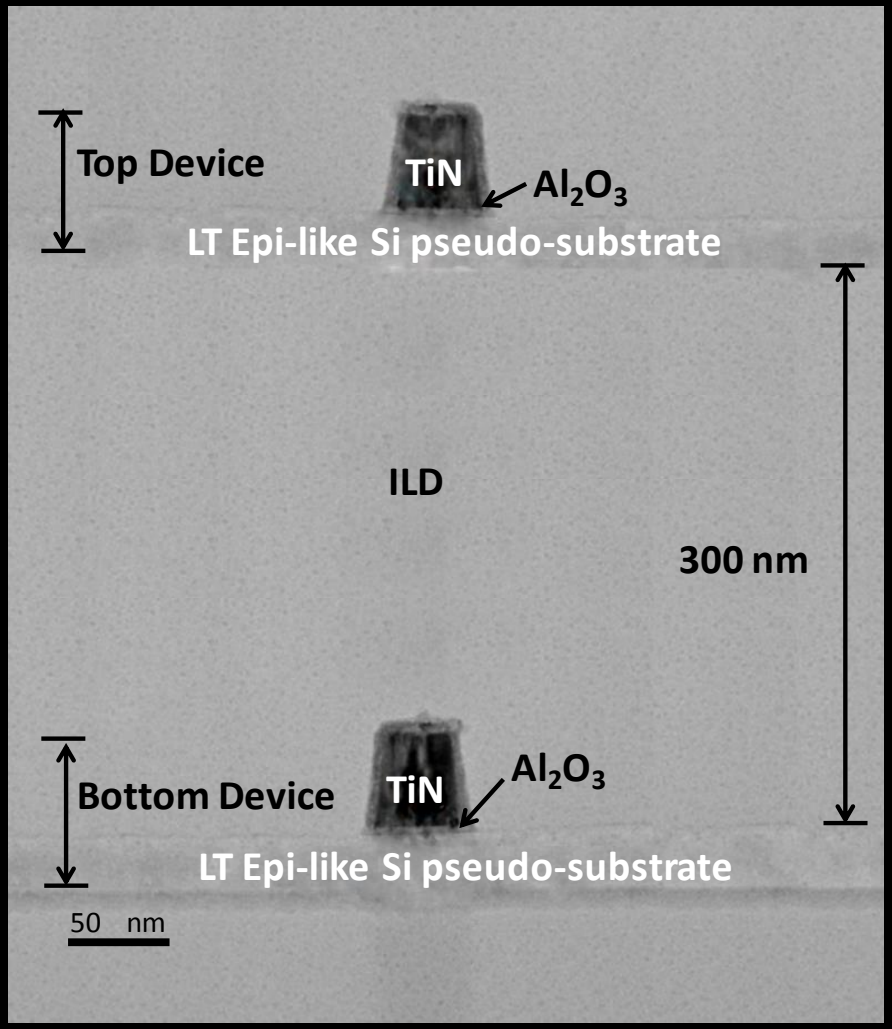
Solder

3D IC



Nano 2016, W-K Yeh

Monolithic 3D^{+}IC



1. 15nm Si substrate 3D^{+}IC technology.。
2. Planar to 3D high-k / Metal Gate FET.。
3. ILD Oxide thickness ~300nm.
4. Low thermal budget process.

Summary

For More Moore,

- Scaling technology is getting tough especially for Lithography process!
- New material and new structure is necessary to keep Moore's law on-going!

For More than Moore,

- New thinking for specific application using mature VLSI technology can be more flexible to create new market.
- Technology need compatible with Si-base IC technology and low cost.

NARLabs
National Applied Research Laboratories

National Nano Device Laboratories

Wen-Kuan Yeh

Director General

National Nano Device Laboratories (NDL)

NARLabs

Commitment · Passion · Innovation

1988 Founded as “National Sub-micron Device Laboratories”

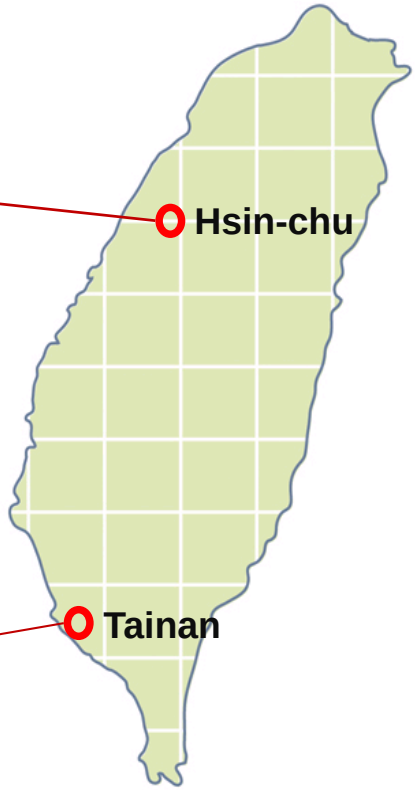
2002 Renamed as “National Nano Device Laboratories”

2003 Affiliated to National Applied Research Laboratories

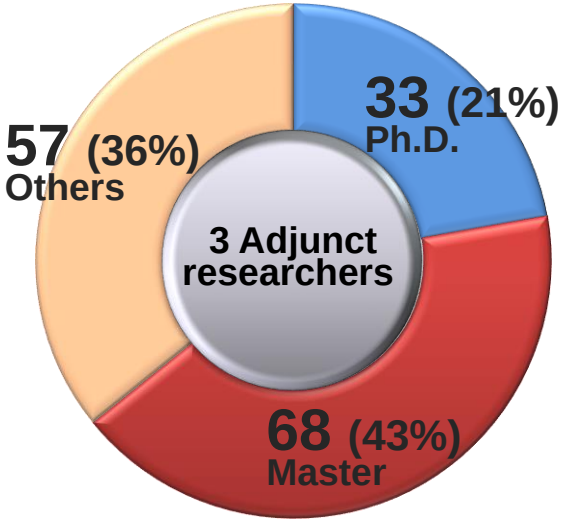
Nanoelectronics-building
(3,500 m^2 cleanroom)

South branch

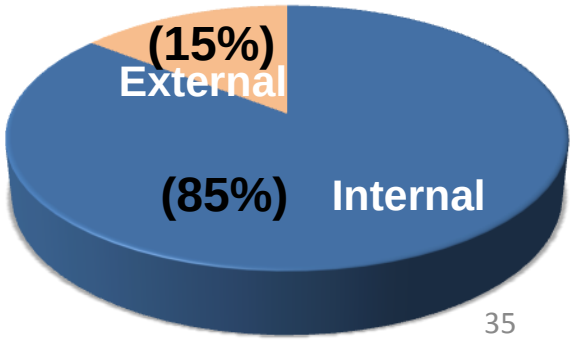
ChiMei Building in NCKU



Staff : 158 members



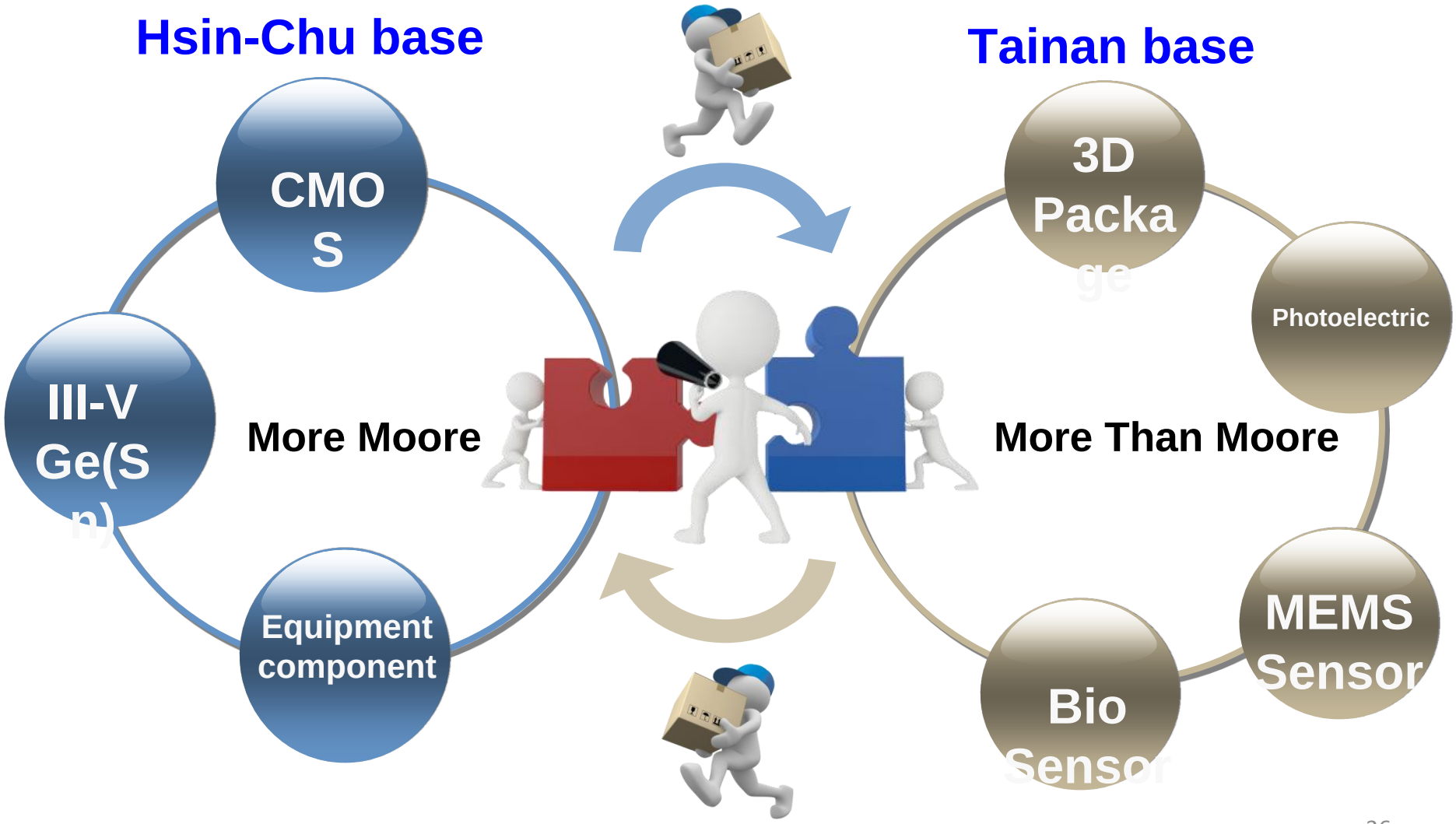
Annual Budget in 2016 ~ USD 20M



Division of NDL labor based on specialization

NARLabs

Commitment · Passion · Innovation



NDL's Core Facilities

NARLabs

Commitment · Passion · Innovation

Nano Device

ALD
Microwave
UHVCVD
RPCVD

CMOS devices

Emerging devices

Advanced Device

Laser anneal
Sputter
HDPCVD
ICPCVD
VHF-PECVD

Core Facilities of Nano Fabrication

6" IC line
8" CMOS line
E-beam Lith.
FIB
Ion implanter
HDPCVD
PVD
CMP

ISO9001:2008

HF Technology

220GHz
RF/MW/mmW
Measurement
platform

Measurement

Verification

ISO 17025

Metrology

HR-TEM
SIMS
XRD
XPS

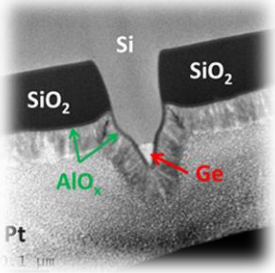
NDL Labs

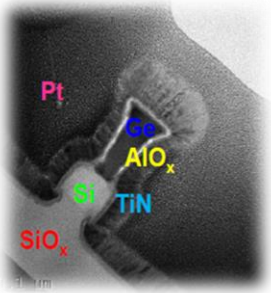
NDL¼v¤ù-0824-pc.wmv - ±1®|

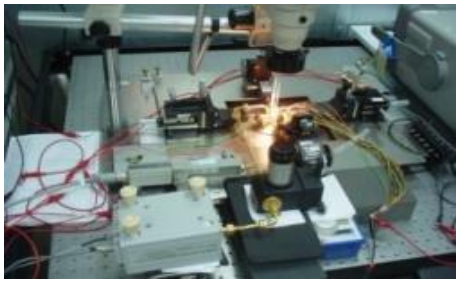
Class 10-100 Clean Room

NARLabs

Commitment · Passion · Innovation







Value Proposition

NARLabs

Commitment · Passion · Innovation

Universities

Research Institutes

Support university and industry to enter technology and advanced materials for emerging device .

IC Fabs

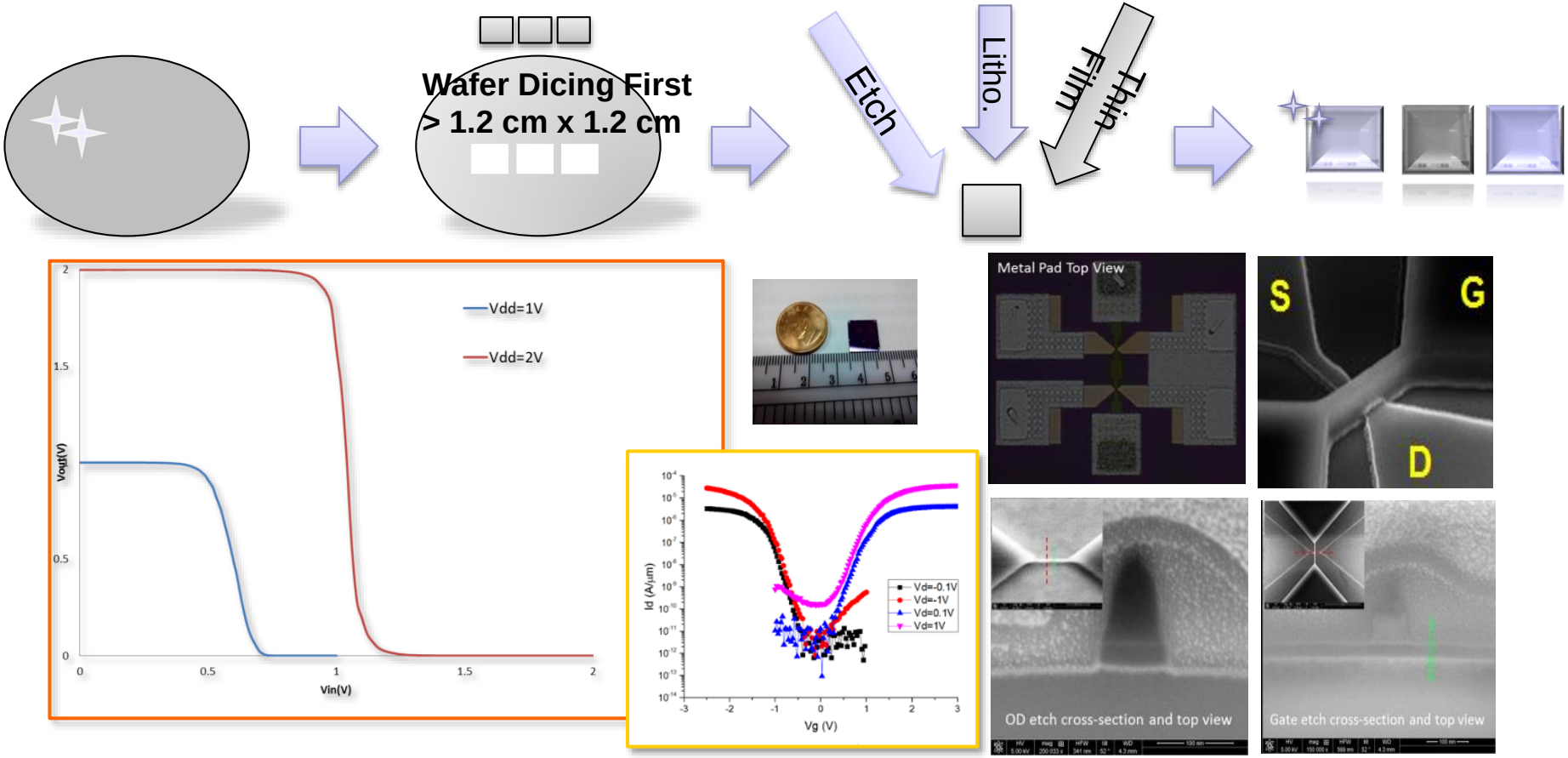
Set up system to provide use-friendly and effective service for University and industry.

Equipment Manufacturers

Chip/Die level Nano-Material based Device Platform - *Multi-Lithography*

NARLabs

Commitment · Passion · Innovation



- NDL's chip/die process is compatible with 65nm standard CMOS fabrication process.
- Optical and e-beam mix-matching could provide accuracy in multi-layer/mask-fabrication for CMOS or CMOS-compatible devices.

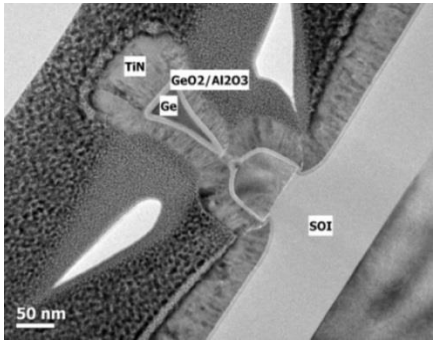
Alternative Material/Structure Device

NARLabs
Commitment · Passion · Innovation

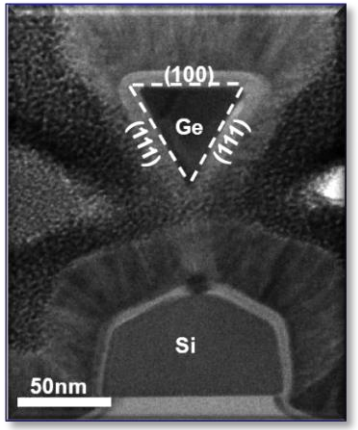
Ge

III-V

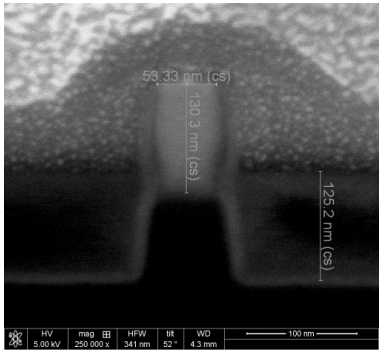
Ge GAA PFETs



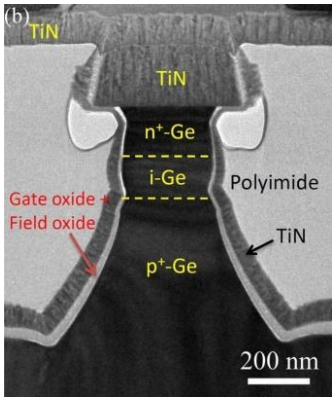
Ge GAA NFETs

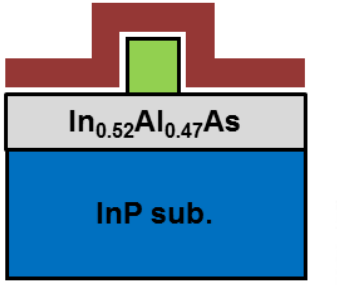


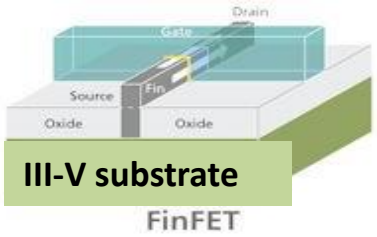
Regrown Ge FinFET

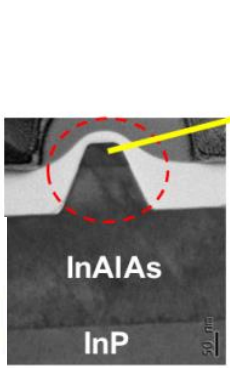


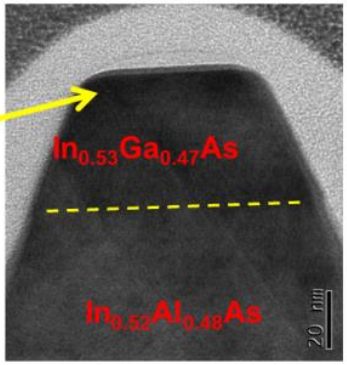
Vertical Ge TFETs

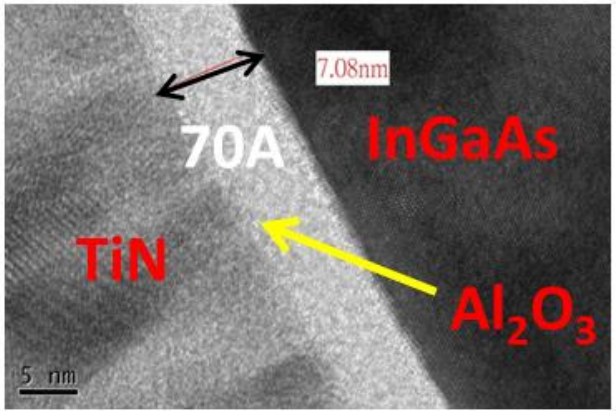








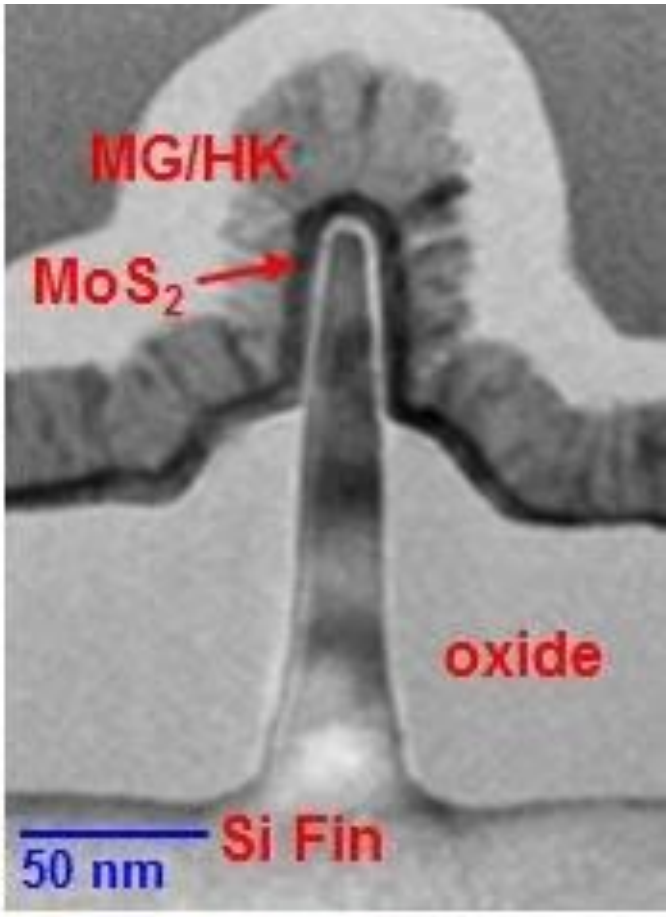




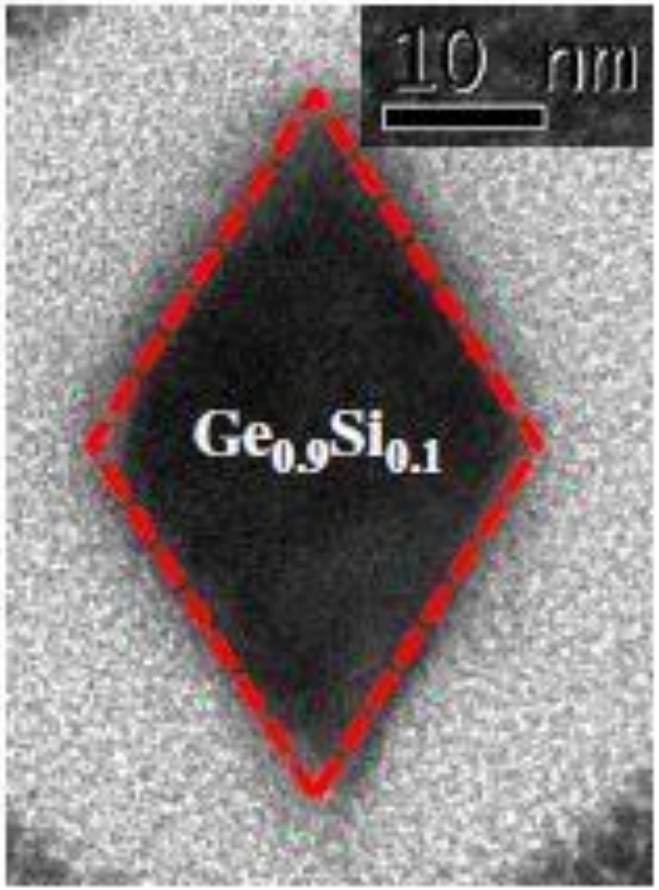
Alternative Material/Structure Device

NARLabs
Commitment · Passion · Innovation

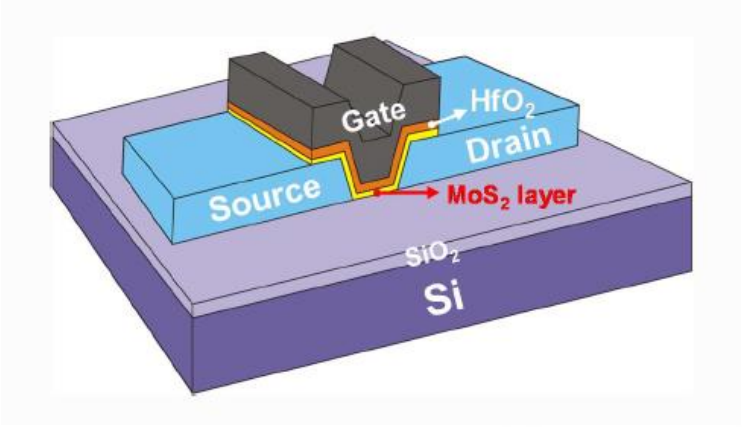
FinFET based 2D FET

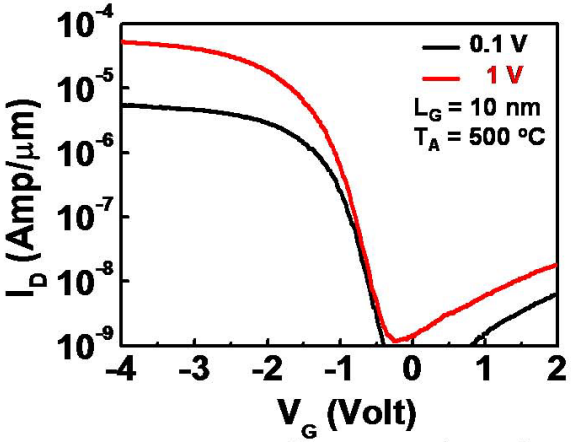


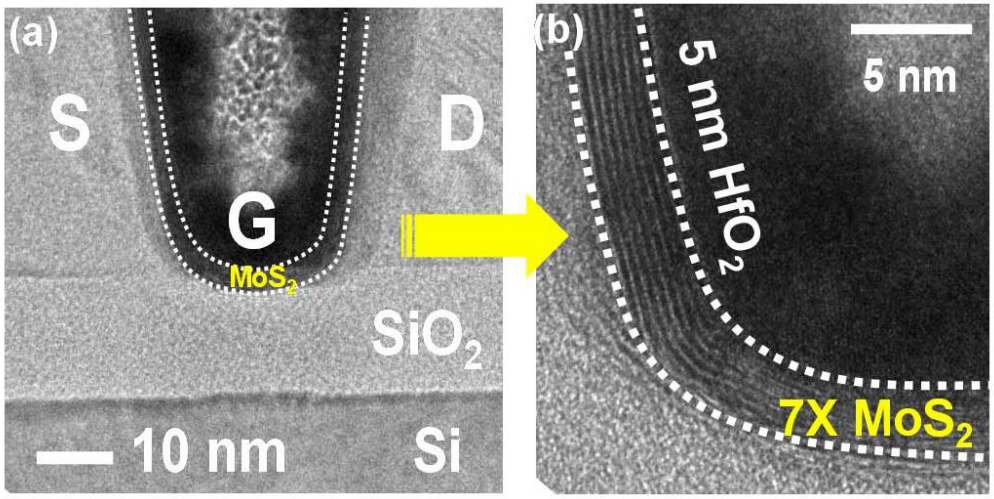
SiGe based GAA FET

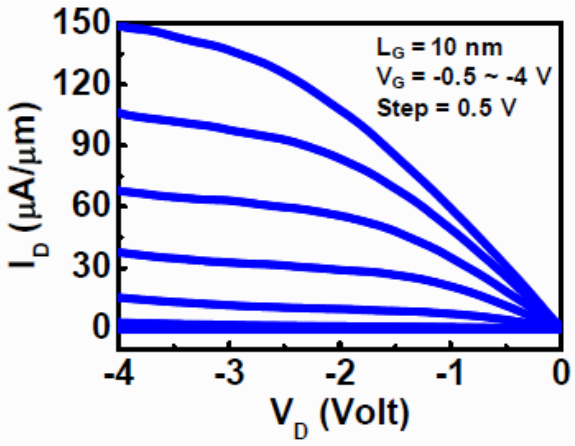


10 nm Lg U-shape MoS_2 FET with Poly-Si Source/Drain Serving Seed









- A U-shape MoS_2 pMOSFET with 10nm channel length
- Poly-Si S/D serves as the nucleation seed for CVD MoS_2

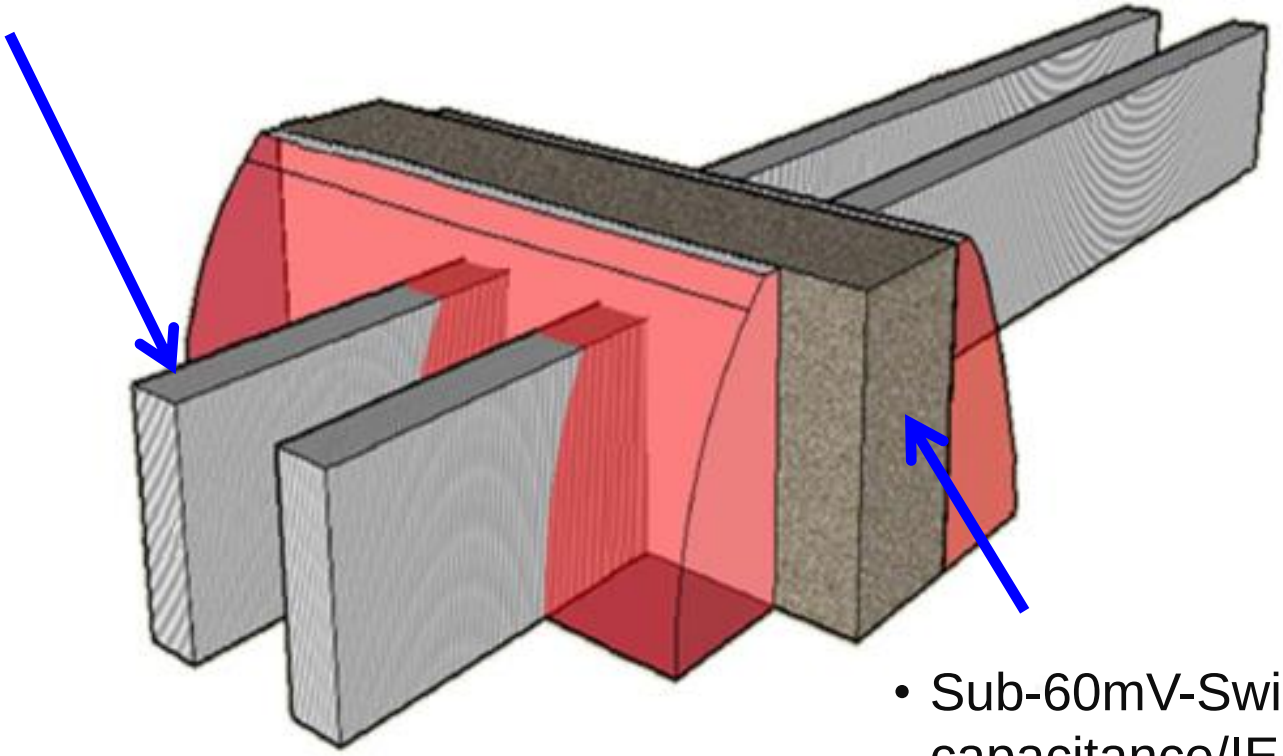
Nano 2016, W-K Yeh

NDL Published at IEDM

for More Moore (2014-15)

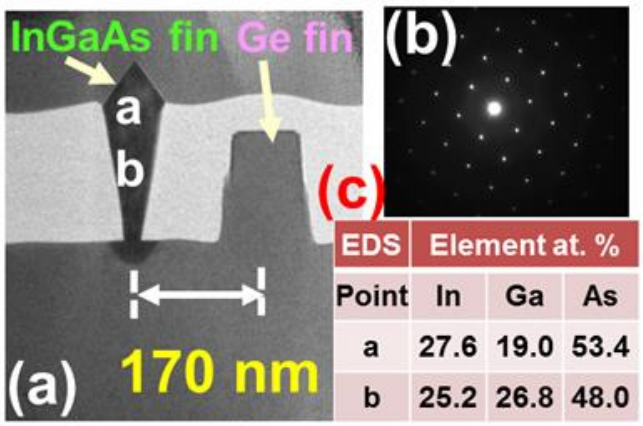
NARLabs

1. **Si-based channel: Sub-5nm shell doping junctionless FETs /IEDM 2104 ~ 2015**
2. **Ge-based channel: Diamond-shaped Ge nanowire by Dry Etch Technology /IEDM 2015 (highlighted paper)**
3. **2D material channel: MoS_2 FinFETs /IEDM 2014 ~ 2015**



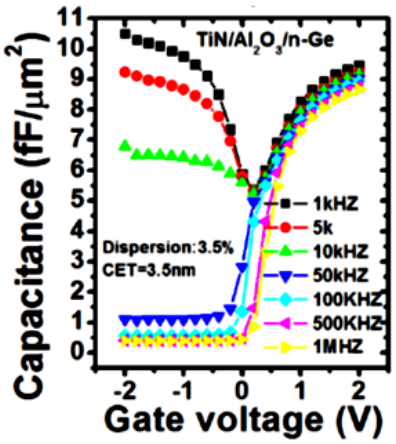
- Sub-60mV-Swing Negative capacitance/IEDM 2015

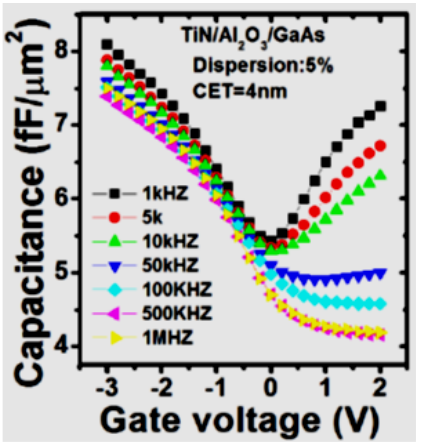
Integration of Ge FIN and III-V FIN on the same Si substrates



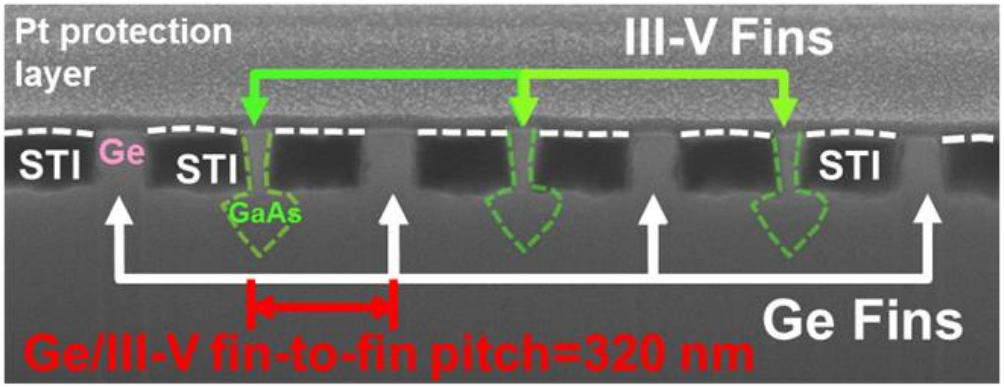
EDS	Element at. %		
Point	In	Ga	As
a	27.6	19.0	53.4
b	25.2	26.8	48.0

InGaAs Fin structure co-integrated with Ge fin on Si

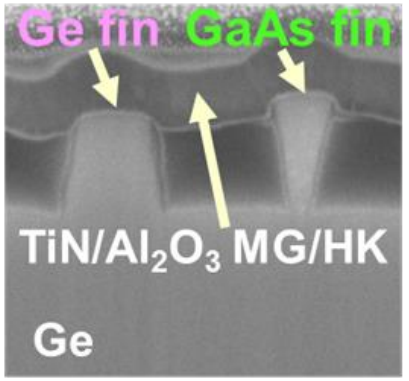




CV characteristics of n-Ge MOS and p-GaAs MOS with the same Al2O3 ALD process.



The interdigitated GaAs/Ge fins formed by etching and selective epi. The surface was flatted by mechanical polish.



Fully integrated GaAs and Ge fins with common HK/MG stack around the 3D fin surface

Nano 2016, W-K Yeh

Steep Slope Transistors - *NC FinFET*

NARLabs

Commitment · Passion · Innovation

Sub-60mV-Swing Negative-Capacitance FinFET without Hysteresis

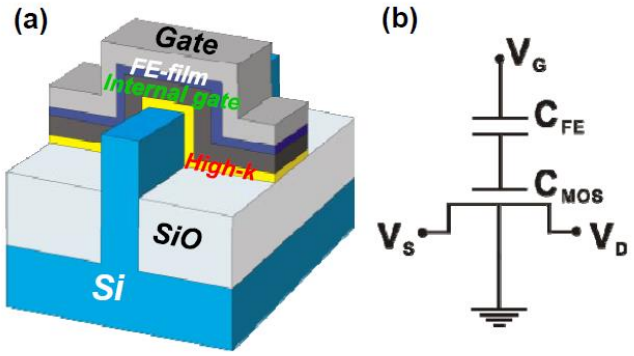


Fig. 1: (a) Schematic structure of NC-FinFET (b) The capacitance network of C_{FE}, C_{MOS} determines the voltage gain.

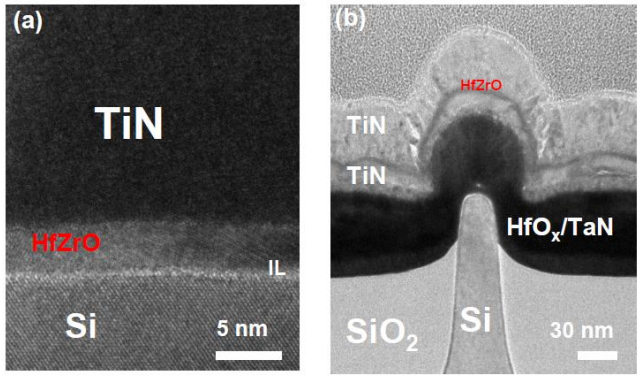


Fig. 4: TEM of (a) planar HfZrOx test capacitor and (b) NC-FinFET with TiN internal gate, HfZrO FE film and TiN gate.

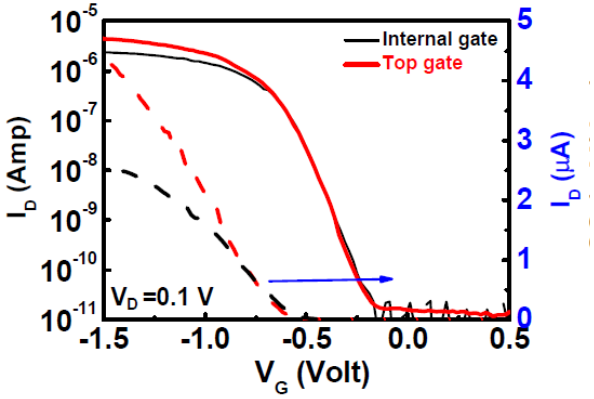


Fig. 12: I_D-V_G of P-type NC-FinFET and of the internal FinFET after 600C anneal (shift to match I_{off}).

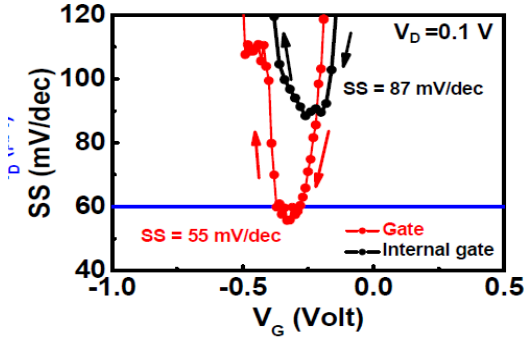


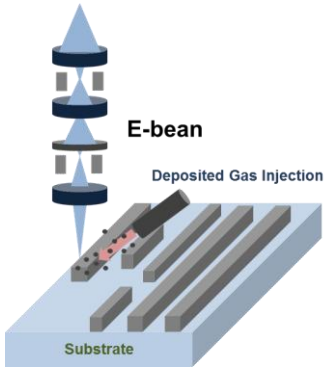
Fig. 13: Comparison between subthreshold swing, SS, of P-type NC-FinFET and internal FinFET.

New Memory:
Sub-10nm and 3D Stack RRAM

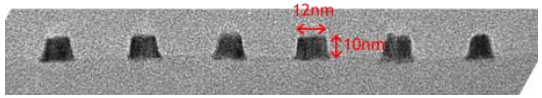
NARLabs

Commitment · Passion · Innovation

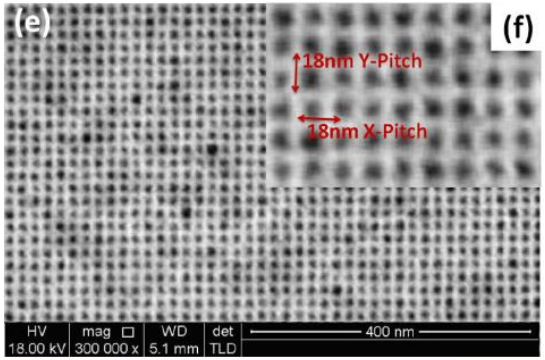
Nano injection Lithography (NIL)



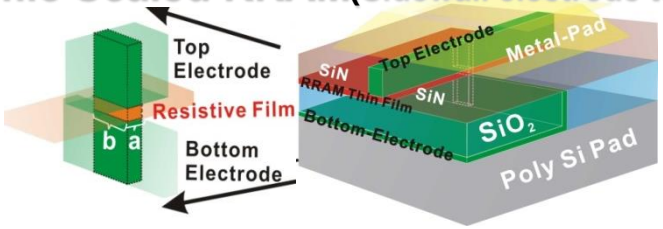
10 nm metal line cross section

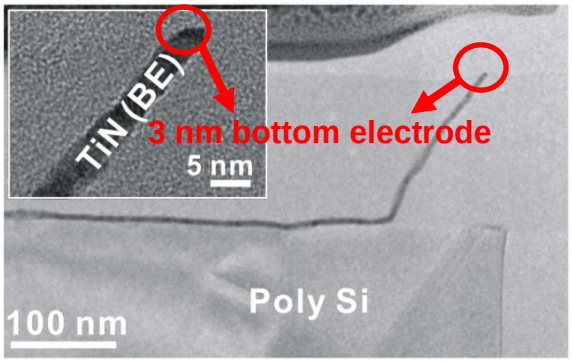


Sub-10 nm RRAM Cell Array

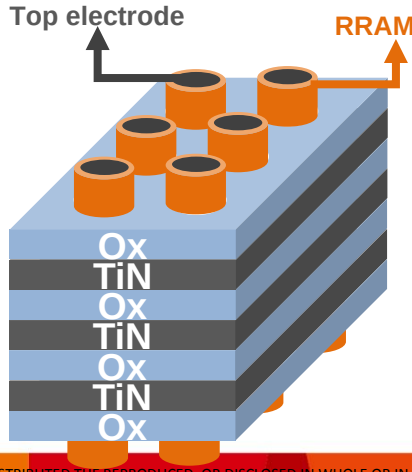


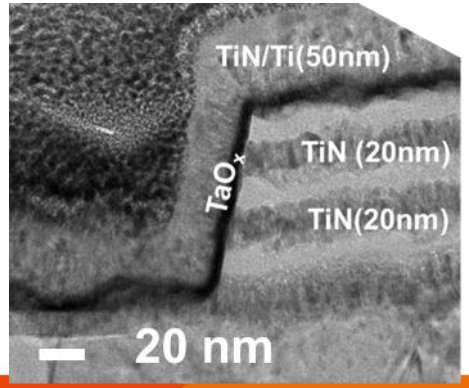
Atomic Scaled RRAM(Sidewall electrode technology)





3D Stack Vertical RRAM





NDL Published at VLSI

NARLabs

Commitment · Passion · Innovation

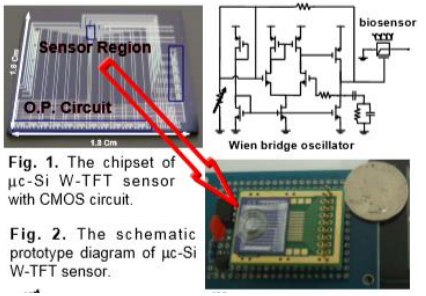
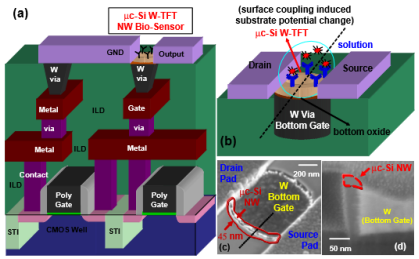
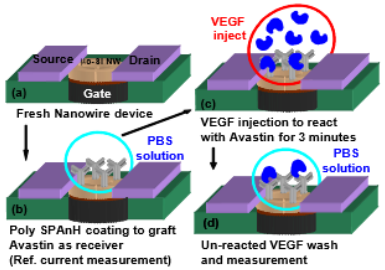


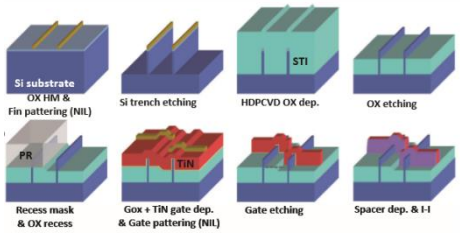
Fig. 1. The chipset of μc-Si W-TFT sensor with CMOS circuit.

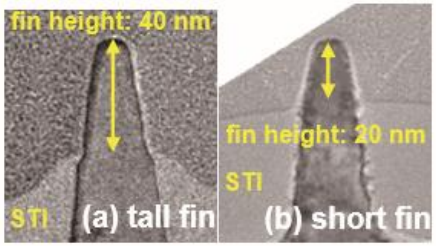
Fig. 2. The schematic prototype diagram of μc-Si W-TFT sensor.

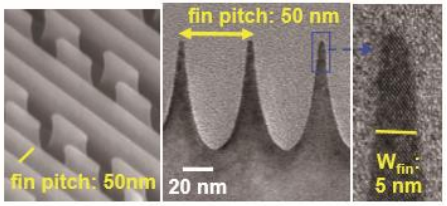




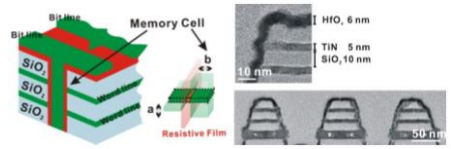
Sub-fM DNA Sensitivity by Self-Aligned Maskless Thin-Film Transistor based SoC Bioelectronics

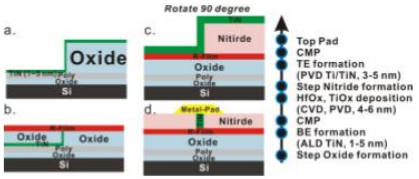


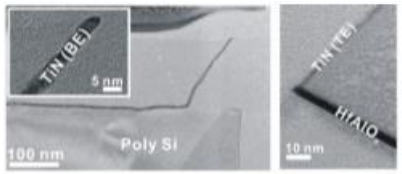


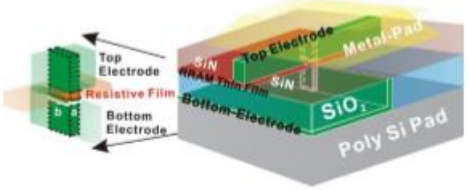


A 10 nm Si-based Bulk FinFETs 6T SRAM with Multiple Fin Heights Technology for 25% Better Static Noise Margin

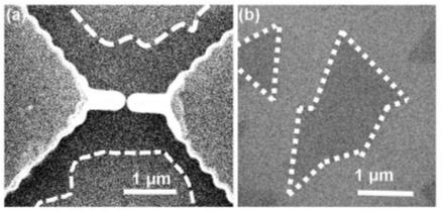


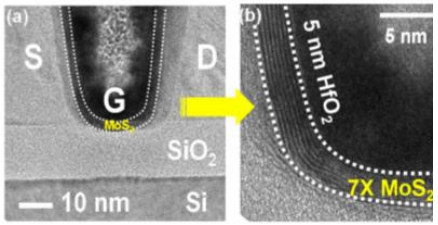


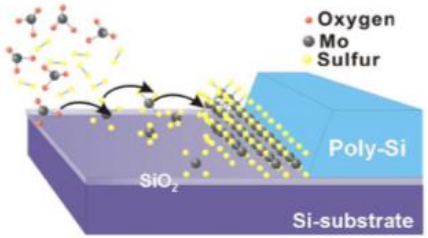




Utilizing Sub-5 nm Sidewall Electrode Technology for Atomic-Scale Resistive Memory







MoS_2 U-shape MOSFET with 10 nm Channel Length and Poly-Si Source/Drain Serving as Seed for Full Wafer CVD MoS_2 Availability

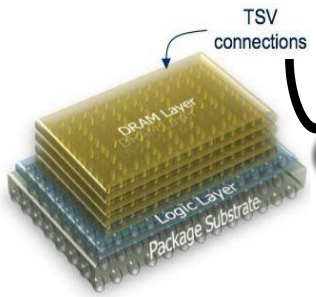
2012 2013 2014 2015 2016

New Integration:
Monolithic 3D+IC Technology

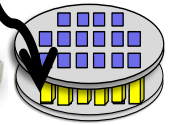
NARLabs

Commitment · Passion · Innovation

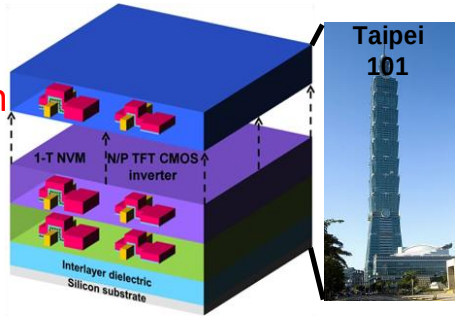
Packaged 3D IC



solution



Multilayered 3D+ IC

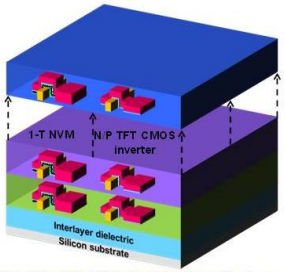


Low cost, high-speed, high-density IC.

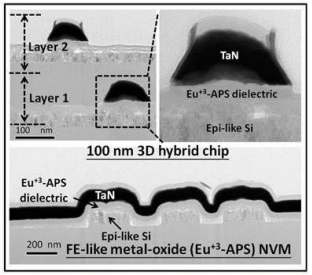
2012 IEEE IEDM S33P6

3D Ferroelectric-like NVM/CMOS Hybrid Chip by sub-400 °C Sequential Layered Integration

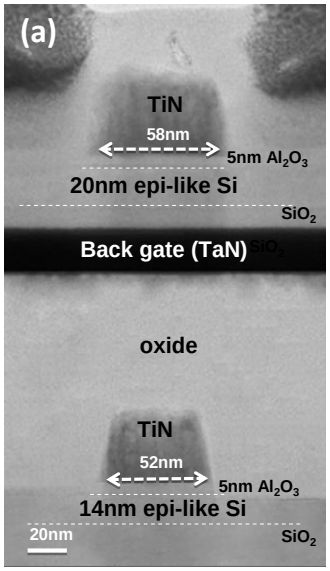
Yu-Chung Lien[1], Jia-Min Shieh[1,2*], Wen-Hsien Huang[1], Wei-Shang Hsieh[1], Cheng-Hui Tu[2], Chieh Wang[2], Chang-Hong Shen[1], Tung-Huan Chou[1], Min-Cheng Chen[1], Jung Y. Huang[2], Ci-Ling Pan[3], Yin-Chieh Lai[2], Chenming Hu[4], and Fu-Liang Yang[1]



3D NVM/CMOS Chips

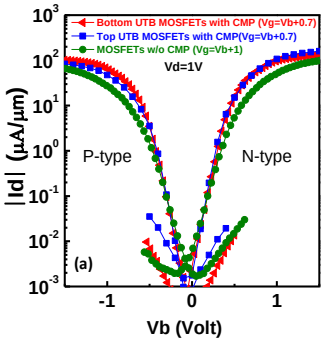


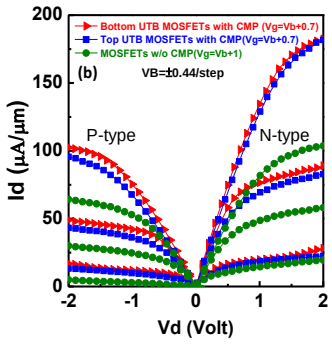
Sequential 3D Hybrid Chips



IEDM2013, s29p6.

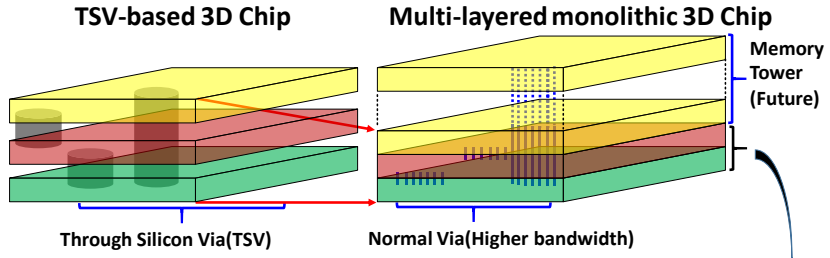
Record-high 121/62 μA/μm on-currents 3D stacked epi-like Si FETs with and without metal back gate



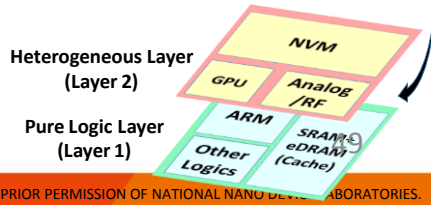


IEDM2013, s9p3.

Monolithic 3D Chip Integrated with 500ns NVM, 3ps Logic Circuits and SRAM



selected as publicity materials for the conference



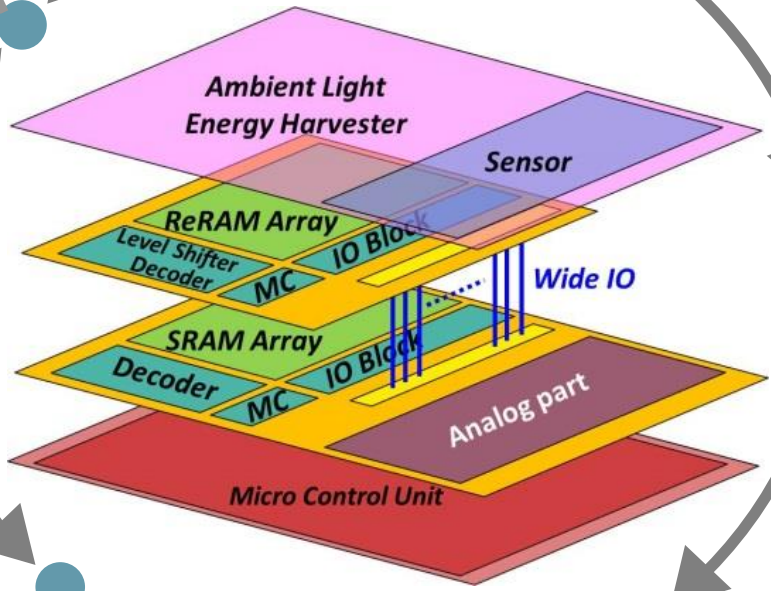
Multi-functional IoT Chips

NARLabs

Commitment · Passion · Innovation

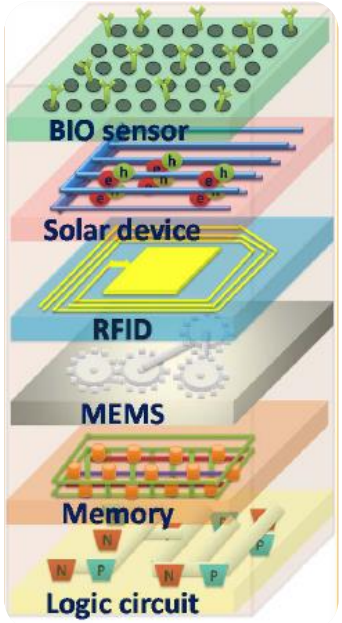
Low Power IC
(Stackable UTB CMOS)

Embedded Memory
(SRAM, ReRAM)



Sensors
(CO Gas Sensor)

Future 3DIC



Communication
(GSM,LTE, WiFi, Mesh Network,etc)

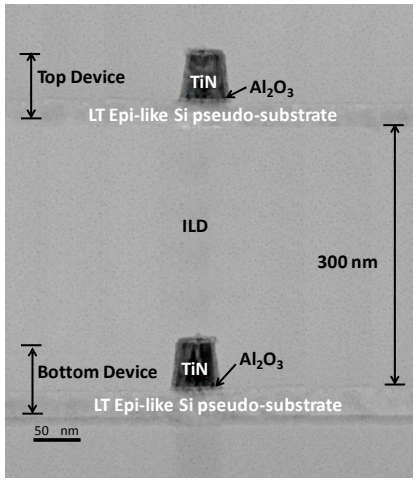
Power Management
(Thin Film Energy Harvester)

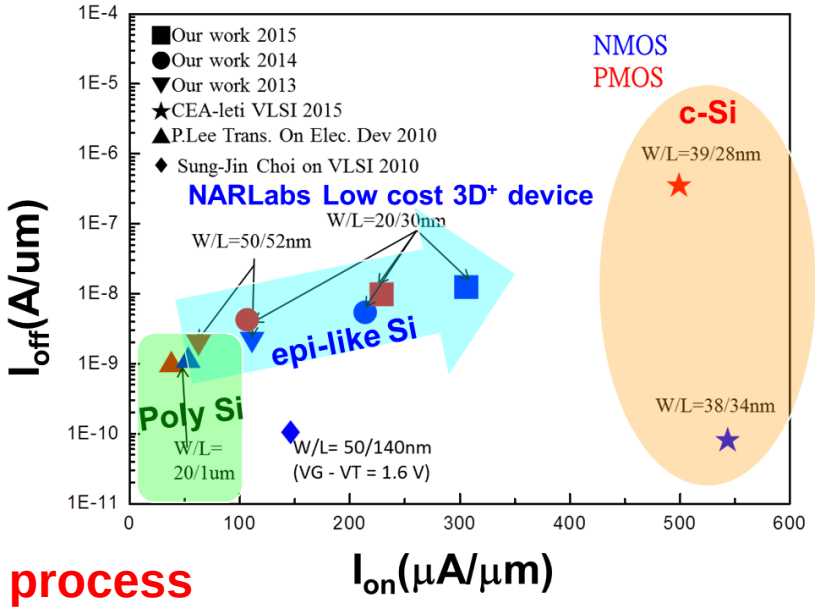
Low Cost 3D+ Device

NARLabs

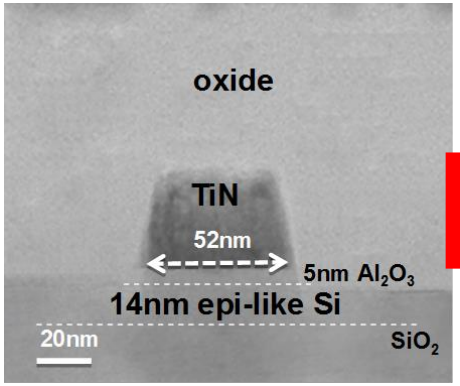
Commitment · Passion · Innovation

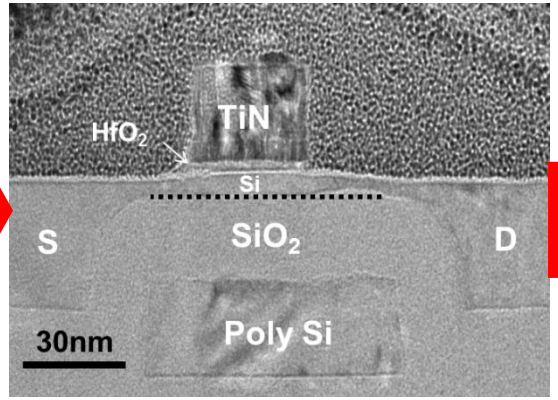
2013~2015 IEDM 3D+ device

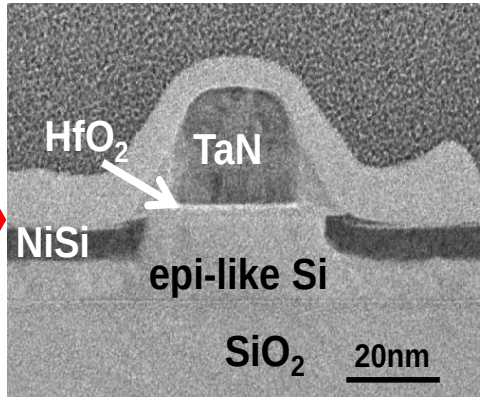




Achieved by low thermal budget laser process







2013 IEDM 3D+ UTB

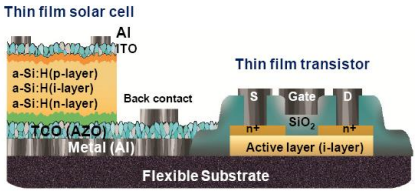
2014 IEDM e-S/D FET

2015 IEDM Nanowire FET

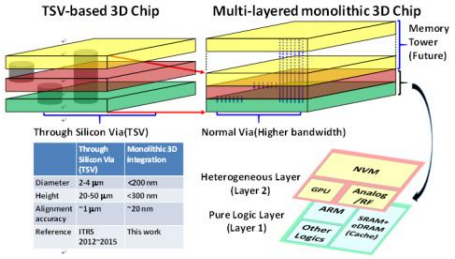
NDL 3D⁺ IC Milestone - Published at IEDM

NARLabs

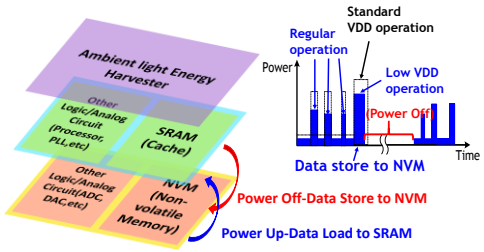
Commitment · Passion · Innovation



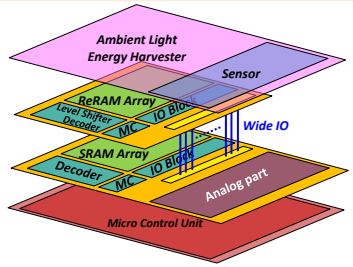
Novel 140°C Hybrid Thin Film Solar Cell/Transistor Technology (2010-IEDM)



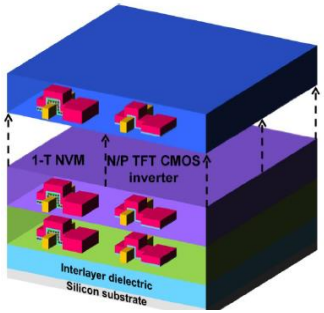
Monolithic 3D Chip integrated NVM, logic circuit and SMAM (2013-IEDM)



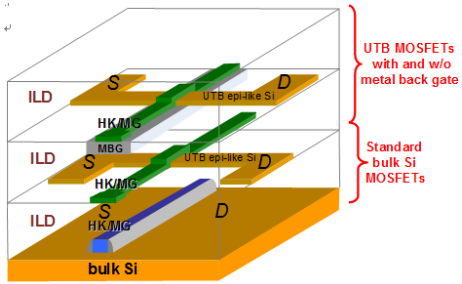
Ge/Si monolithic 3D-IC with stacked SiGeC ambient light harvester (2014-IEDM) (High-light paper)



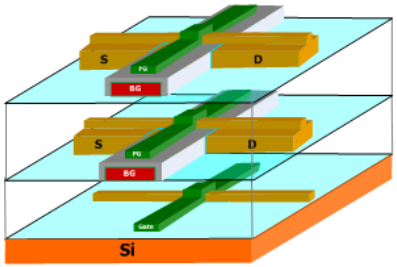
TSV-free Monolithic 3D-IC with Heterogeneous Integration for IoTs (2015-IEDM) (High-light paper)



3D Ferroelectric-like NVM/CMOS hybrid chip (2012-IEDM)



Recorded-high on currents 3D stacked epi-like Si FETs (2013-IEDM)



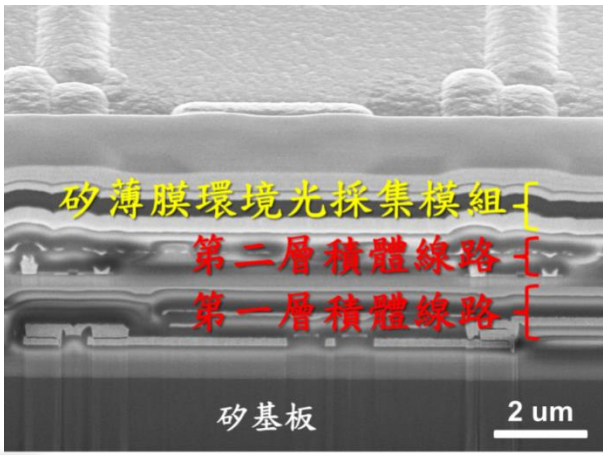
V_{th} adjustable stacked Si/Ge-FETs (2014-IEDM)

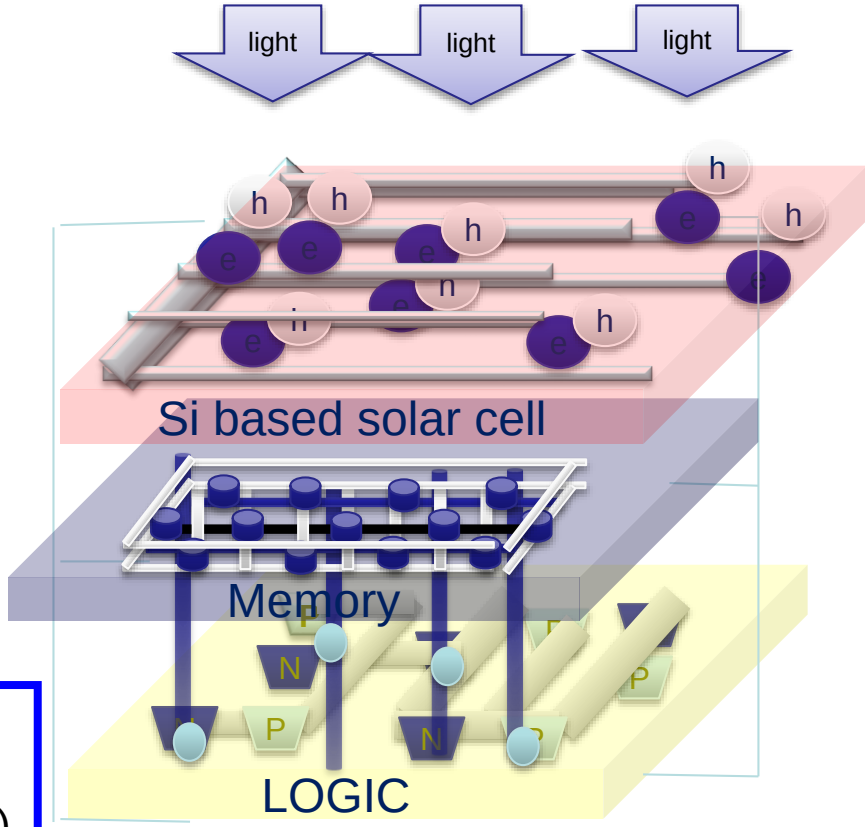
Monolithic 3D⁺ nanoelectronics for IoTs Using Local and Selective FIRLA Technology (2015-IEDM)

2010-2012 | 2013 | 2014 | 2015

Self-power application

Integrate Solar cell, Memory and Logic circuit!





PV Tag

Battery-less Photovoltaic RF Tag
3D-positioning demonstration
under Indoor Environment (600lux)

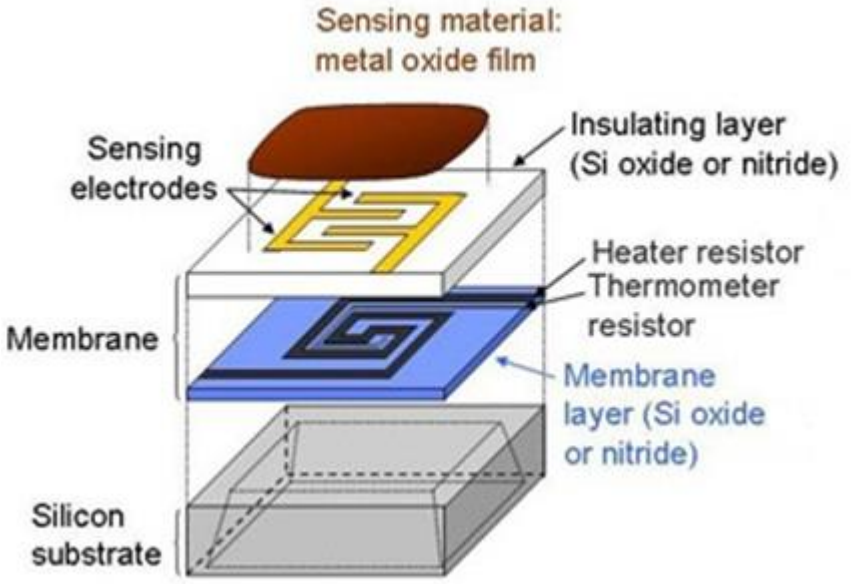
Solar, in-house light

Self power IoT

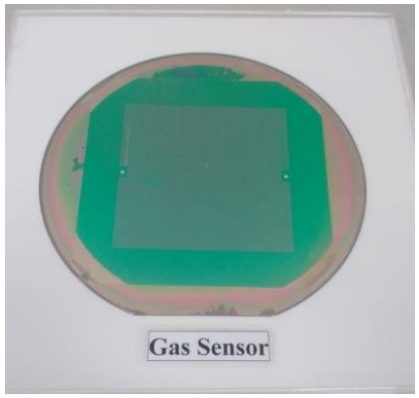
Nano 2020, ... Yeh

Power Gas Sensor Platform

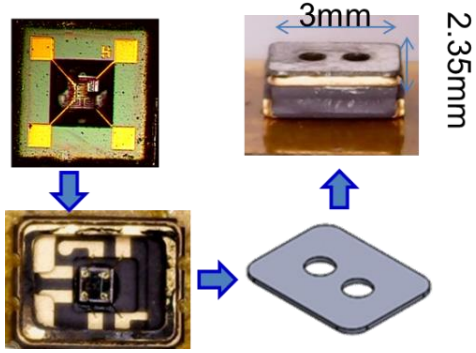
NARLabs



CO & CO_2 (self-assembly)

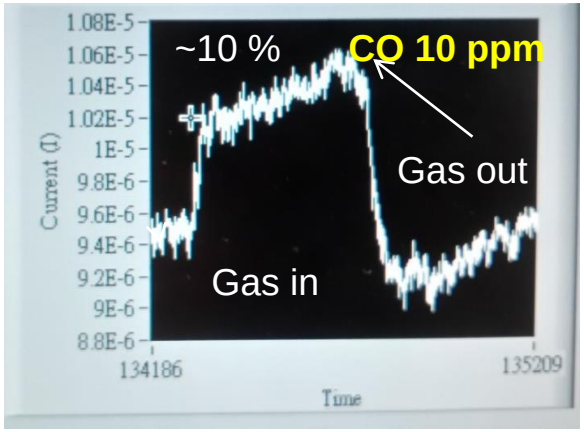


Package



Alcohol sensor

CO sensor in Smart phone (self-assembly)



Rapid screening detection sensor
- Pathogens

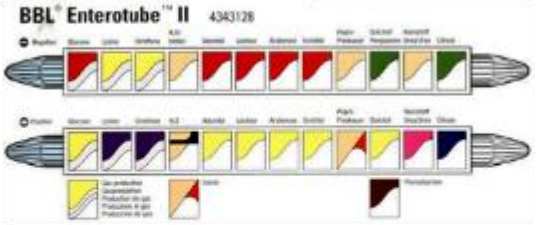
承諾·熱情·創新

Traditional

Bacteria detection in hospital

Blood culture
bacterial concentration
(>10^9 CFU / ml)
24-48 hr

Plate culture
24 hr

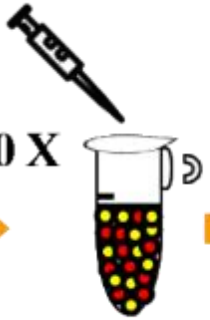


Biochemical Detection
(Enterotube II)
16-24 hr

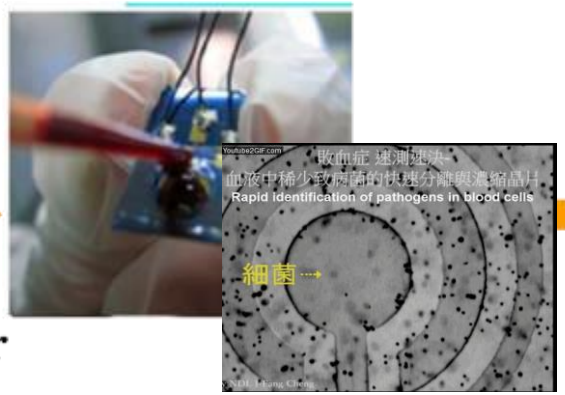
NDL

Blood culture
bacterial concentration
(>10^5 CFU / ml)
4 hr

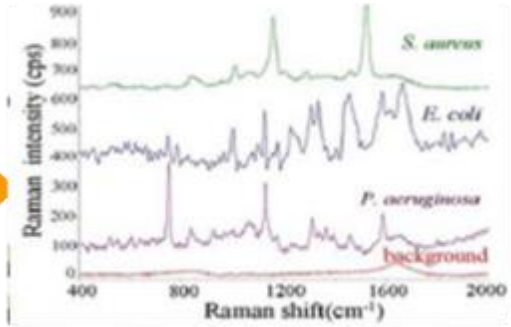
Dilute 20 X



Prepared buffer
+AgNPs
1 min



Electrokinetically trapping
3 min

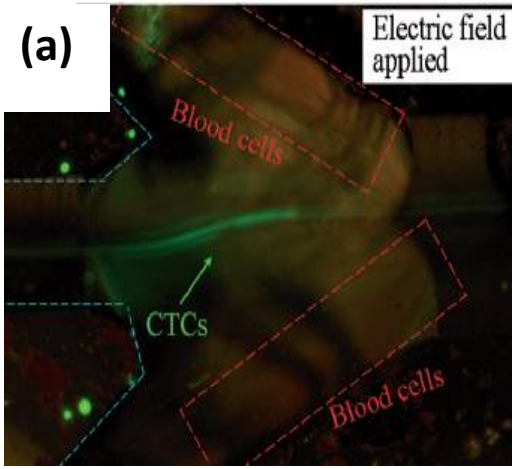


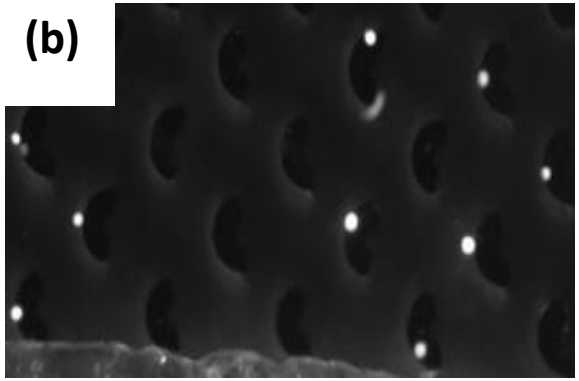
Raman Spectroscopy
~15 sec

Rapid screening detection sensor - Cancer

承諾·熱情·創新

* Rapid: ~2 hr isolation time
* High purity
* High recovery: > 80%





(a) Lung adenocarcinoma cells and blood cells separated from the resulting image in the micro- flow channel , (b) A single- cell lung cancer is to catch up with the micro- structure of the positioning result, and (c)published on a Chip as a Back Cover。

Metrology Analysis Service

NARLabs

承諾・熱情・創新

Nano Metrology Laboratory

Audited by Taiwan Accreditation Foundation (TAF)

Quality Management System

Technical Management System

AFM	SEM	TEM	SIMS	XPS	XRD
Step Height Line width	Line width Surface Image Observation	Line width	Depth Profile for Boron	Surface Qualitative	Phase Identification

International Laboratory Accreditation Cooperation (ILAC) Mutual Recognition Arrangement

Our technical capabilities have reached international standards and commensurable techniques with other 60 accredited laboratories in 73 countries over the world.

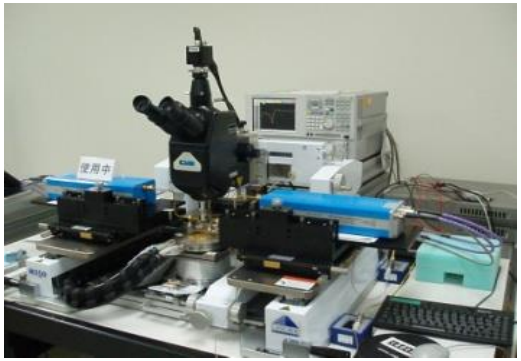
High-Frequency Measurement Capability

NARLabs

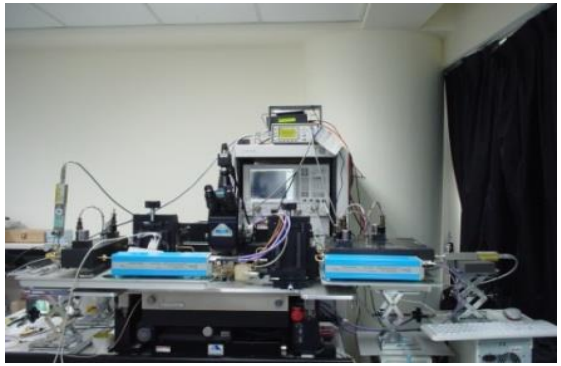
Commitment · Passion · Innovation

Comprehensive measurement services for high-speed/high-frequency devices and circuits up to 220 GHz

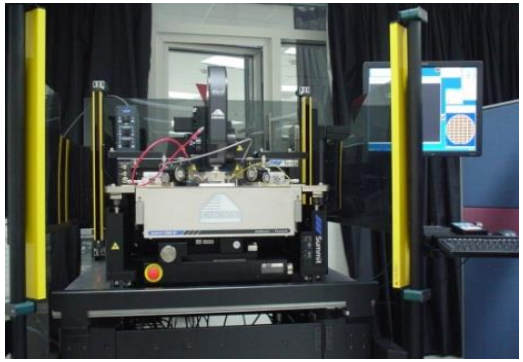
- RF/MW/mmW Circuit Measurement up to 220 GHz
- S-parameter Measurement up to 500 GHz
- Noise Parameter Measurement up to 90 GHz
- Load-Pull Measurement up to 94GHz
- High Voltage/High power Device and Circuit Measurement



220 GHz S-parameters Measurement System



60-90 GHz Noise/Load-Pull Measurement System



High Power Device Measurement System, up to 3000 V, RT to 200 ℃

Cooperation with Research Team

New Structure

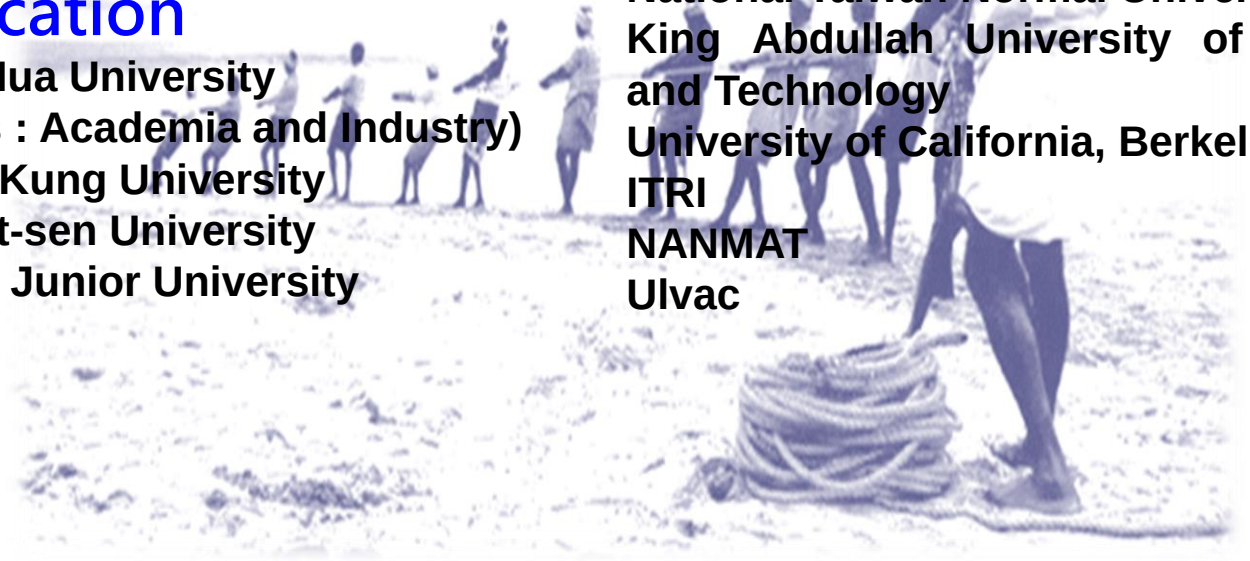
National Chiao Tung University (I-RiCE)
National Taiwan University
National Tsing Hua University
National Sun Yat-sen University
University of California, Berkeley
Tohoku University
TSMC
UMC

New Application

National Tsing Hua University
(Minor Alliances : Academia and Industry)
National Cheng Kung University
National Sun Yat-sen University
Leland Stanford Junior University
MXIC
AUO
Motech
Liteon
Foxconn

New Material

National Taiwan University
(Major Alliances between Academia and Industry)
National Chiao Tung University (I-RiCE)
National Tsing Hua University
National Cheng Kung University
(tsmc-NCKU R&D Center)
National Central University
National Taiwan Normal University
King Abdullah University of Science and Technology
University of California, Berkeley
ITRI
NANMAT
Ulvac



Possible Cooperation Topic

NARLabs
承諾·熱情·創新

Nano-Devices

- Ge/SiGe and III-V FinFETs & Nanowire/ GAA FETs.
- 2D FET (MoS_2, WSe_2, Graphene, Silicene), Spintronic.

Process Technologies

- Low temperature activation (MW, laser)/ contact/ Junctionless
- high-k material /Metal Gate
- Monolithic 3D CMOS/ heterostructure Integration.
- RRAM, MEMS, solar cells, photonic, bio-chips (Si substrate).
- Ambient charger (light, heat, vibration, microwave).

Equipment and materials

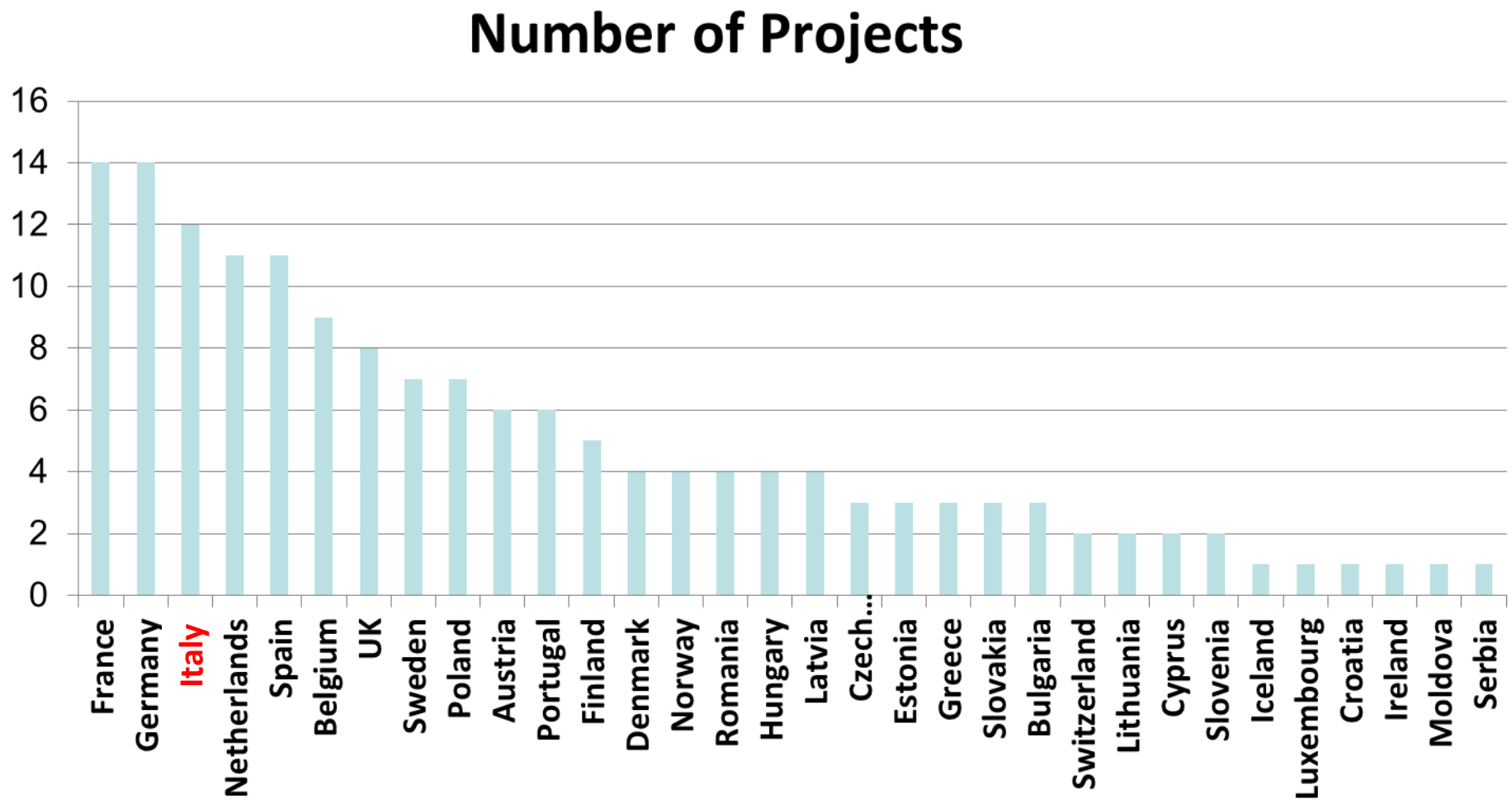
- Joint development.
- Test and evaluation.

International training program

Why Partner With Taiwan

- Fully eligible to participate in Horizon 2020
- Bring funding from Taiwan
- Contributes unique expertise into the projects
- Access to markets and networks in Asia-Pacific

Taiwan's H2020 Partner Countries



Nano 2016, W-K Yeh

Find Partners in Taiwan

NCP Taiwan website: https://www.ncp.tw/en/

Find Partners in Taiwan by H2020 Research Area:
https://www.ncp.tw/en/faq/

NARLabs

Commitment · Passion · Innovation

Thanks for your attention !